

# ZMCMT83085/ZMCMT83087

## ZMCMT83085/ZMCMT83087 High Reliability Isolated Half-Duplex RS-485 Transceivers

### 1 Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL recognition: up to 5000Vrms for 1 minute per UL1577
  - CSA component notice 5A
  - CQC approval per GB4943.1-2011
- Up to 5000Vrms Insulation voltage
- Bus side power supply voltage: 3.0V to 5.5V
- VDD1 supply voltage: 2.5 to 5.5 V
- High CMTI:  $\pm 200\text{Kv/us}$
- High system level EMC performance:
- Bus Pins meet IEC61000-4-2  $\pm 12\text{ kV ESD}$ 
  - Other Pins meet  $\pm 7\text{ kV contact ESD}$
  - Operation temperature:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Fail-safe protection receiver
- Slew rate limitation
- Robust isolation barrier life:
  - More than 40-year projected lifetime
- Up to 256 transceivers on the bus
- RoHS-compliant packages: SOIC 16 (wide body)

### 2 Applications

- Industrial automatic control
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

### 3 Description

ZMCMT83085/ZMCMT83087 is a high reliability isolated half duplex RS-485 transceiver based on CMOSTEK digital isolation technology. It is safety certified by UL1577 support 5kVrms insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The Bus pins of ZMCMT83085/ZMCMT83087 is protected from  $\pm 12\text{kV}$  system level ESD to GND2 on Bus side. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

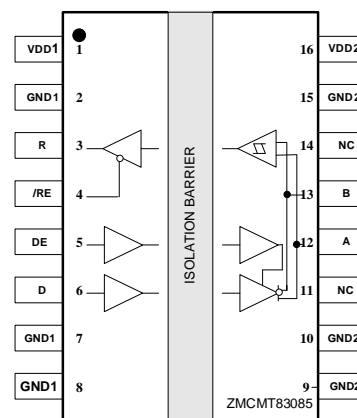
The data rate of ZMCMT83085/ZMCMT83087 is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

The ZMCMT83085/ZMCMT83087 is available in wide-body (WB) 16-pin SOIC packages.

#### Device Information

Part No.	Package	Body Size (mm x mm)
ZMCMT83085/ ZMCMT83087	WB(W) SOIC-16	10.4 x 7.5
Refer to section 12 for ordering information.		

#### Functional Block Diagram



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## 4 Absolute Maximum Ratings

**Table 1. Absolute Maximum Ratings<sup>[1]</sup>**

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage <sup>[2]</sup>	VDD <sub>1</sub> , VDD <sub>2</sub>		-0.5	6	V
Maximum input voltage	/RE, DE, TxD		-0.4	VDD+0.4	V
Common-mode transients	CMTI		200		kV/us
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ		-7	12	V
Voltage input, transient pulses, A,B,Y and Z (through 100 Ω resistors)	V <sub>IT</sub>		-50	50	V
Receiver output current	IO		-15	15	mA
Maximum surge isolation voltage	VIOSM			8	kV
Operating temperature	T <sub>opr</sub>		-40	125	°C
Storage temperature	T <sub>STG</sub>		-40	150	°C
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V
	HBM (All pins)			±6000	V
	CDM			±2000	V

## 5 Pin Description

The pin list is shown as below.

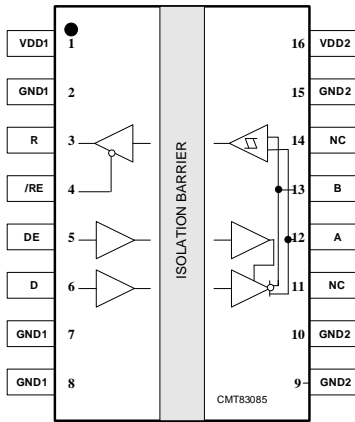


Figure 1-1. ZMCMT83085 Pin List

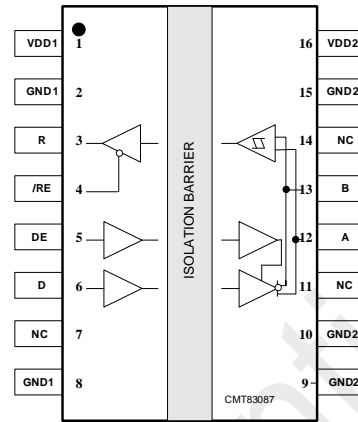


Figure 2-2. ZMCMT83087 Pin List

Symbol	Pin No.		Description
	CMT83085	CMT83087	
VDD1	1	1	Power Supply for Isolator Side 1
GND1	2	2	Ground reference for Isolator Side 1
R	3	3	Receive output
/RE	4	4	Receive enable input. It is a low level input.
DE	5	5	Driver enabled input. It is a high level input
D	6	6	Driver transmitting data input.
GND1	7,8	8	Ground reference for Isolator Side 1
GND2	9,10,15	9,10,15	Ground reference for Isolator Side 2
NC	11,14	7,11,14	No Connection.
A	12	12	Non-inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD1 or VDD2 is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
B	13	13	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD1 or VDD2 is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
VDD2	16	16	Power Supply for Isolator Side 2

## 6 Typical Application

### 6.1 Typical Application Schematic

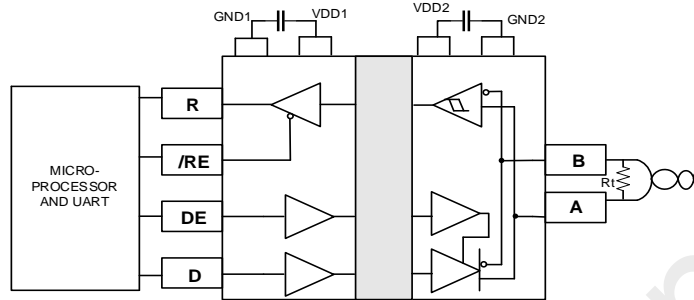
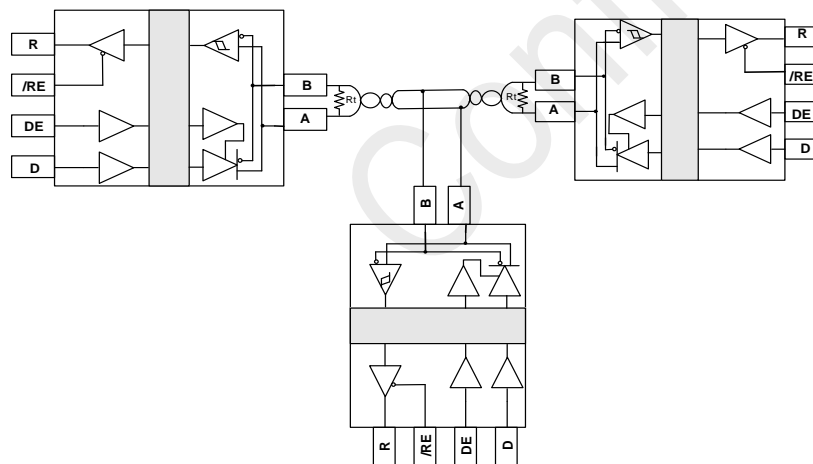


Figure 2. Typical Application Circuit



Note:  $R_t$  is a special matching impedance with typical value of 120  $\Omega$ .

Figure 3. Typical Isolated Half-duplex RS-485 Application

### 6.2 PCB Layout Guidelines

The CMT83085/CMT83087 requires a 0.1  $\mu\text{F}$  bypass capacitor between VDD1 and GND1, 10 $\mu\text{F}$  bypass capacitor between VDD2 and GND2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

## 6.3 ESD Protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handling and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices. Bus pins:

- $\pm 8$  kV HBM.
- $\pm 12$  kV using the Contact Discharge method specified in IEC 61000-4-2

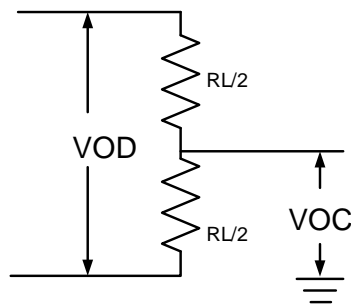
Other pins except bus pins:

- $\pm 6$  kV HBM.
- $\pm 7$  kV using the Contact Discharge method specified in IEC 61000-4-2

## 6.4 256 Transceivers on the Bus

The devices have a 1/8 unit-load receiver input impedance (96k $\Omega$ ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

## 7 Parameter Measurement Circuit Setup



**Figure 4. Driver DC Test Load**

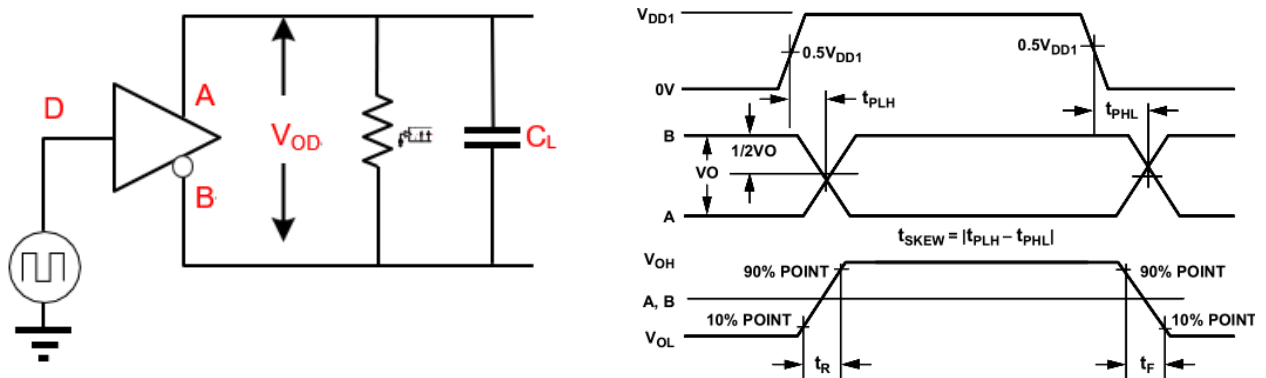


Figure 5. Driver Timing Test Circuit and Waveform

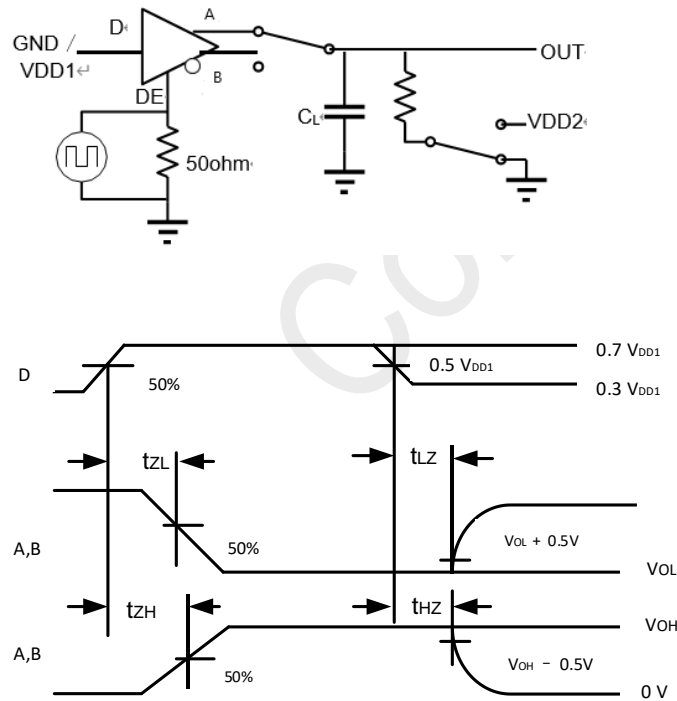


Figure 6. Driver Enable Disable Timing Test Circuit and Waveform

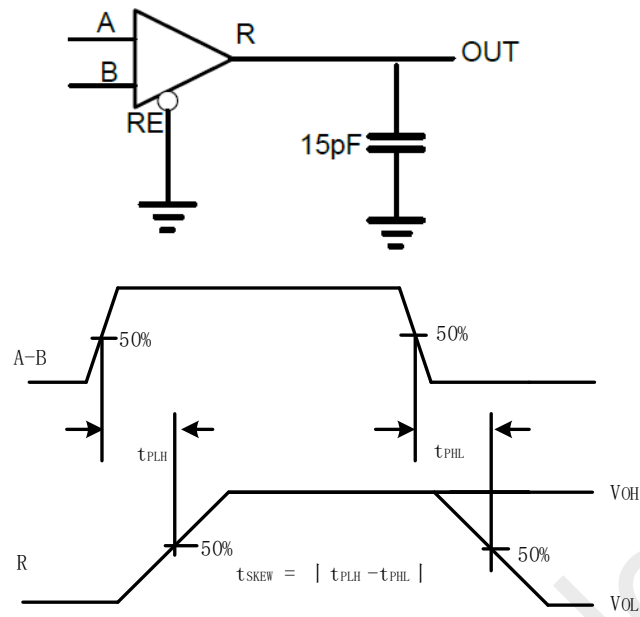


Figure 7. Receiver Propagation Delay Test Circuit and Waveform

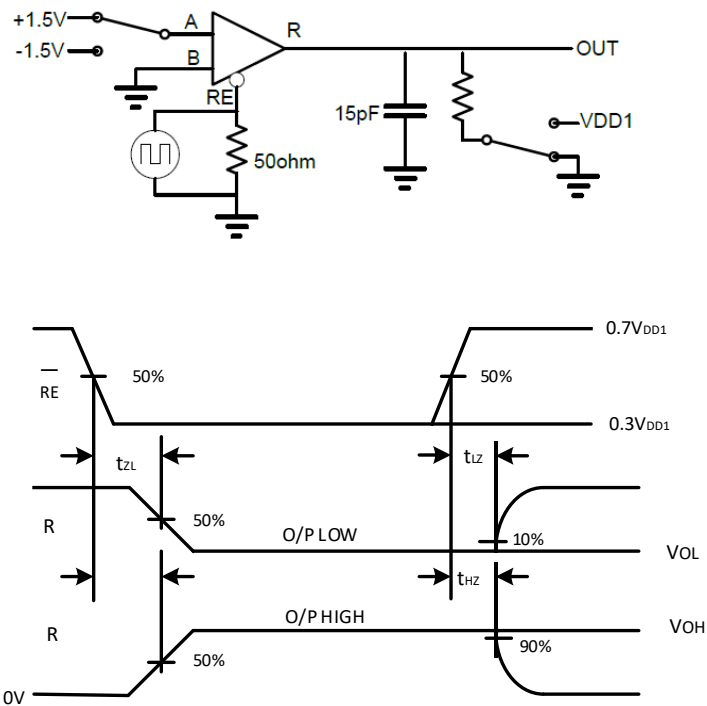


Figure 8. Receiver Enable Disable Timing Test Circuit and Waveform



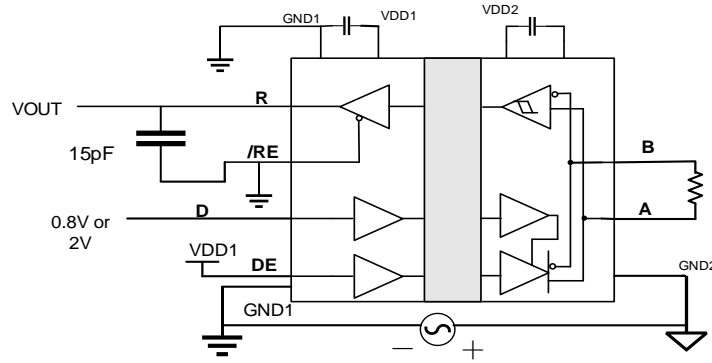


Figure 9. Common-Mode Transient Immunity Test Circuit

## 8 Specifications

### 8.1 DC Electrical Characteristics

VDD1 = 2.5V~5.5V, VDD2 = 3.0V~5.5V, T<sub>A</sub> = -40 to 125 °C. Unless otherwise noted, typical values are at VDD1=5V, VDD2=5V, T<sub>A</sub>=25 °C.

Table 3. Electrical Characteristics

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>DD1</sub>		2.5		5.5	V
	V <sub>DD2</sub>		3.0		5.5	V
Logic side supply current	I <sub>DD1</sub>	VDD <sub>1</sub> = 5 V, DE = high, /RE = D = low, no load		2.85	5.2	mA
		VDD <sub>1</sub> = 3 V, DE = high, /RE = D = low, no load		2.81	5	
Bus side supply current	I <sub>DD2</sub>	VDD <sub>1</sub> = 5 V, DE = high, /RE = D = low, no load		2.1	5	mA
		VDD <sub>1</sub> = 5 V, DE = high, /RE = D = low, no load		2.12	4.5	
Thermal-shutdown Threshold	T <sub>TS</sub>			145		°C
Thermal-shutdown Hysteresis	T <sub>TSH</sub>			15		°C
Common Mode Transient Immunity	CMTI			±200		kV/us
<b>Logic Side</b>						
High level input voltage	V <sub>IH</sub>	DE, D		1.65		V
		/RE		0.8		
Low level input voltage	V <sub>IL</sub>	DE, D, /RE		1.65		V
		/RE		0.8		
Input threshold	V <sub>IT</sub>	Input Threshold at rising edge		1.65		V
	V <sub>IT_HYS</sub>	Input Threshold Hysteresis		0.2		
Input Pull up Current	I <sub>PU</sub>	DI/RE			10	uA

Input Pull down Current	$I_{PD}$	DE	-10			uA
Output Voltage High	$V_{OH}$	$I_{OH} = -4mA$	$V_{DD1} - 0.3$			V
Output Voltage Low	$V_{OL}$	$I_{OL} = 4mA$			0.3	V
Output Short-Circuit Current	$I_{OSR}$	$0 \leq V_R \leq V_{DD1}$			109	mA
Three-State Output Current	$I_{OZ}$	$0 \leq V_R \leq V_{DD1}, /RE = high$	-15			uA
Input Capacitance	$C_{IN}$	DE, D, /RE		2		pF
<b>Driver</b>						
Differential output voltage	$ V_{OD} $	$V_{DD}=5V, TXD=0, R_{load} = 60\Omega$	2.4		VDD2	V
		$R_L=100\Omega$ (RS-422)	3		VDD2	
		$R_L=54\Omega$ (RS-485)	2.2		VDD2	
Change in magnitude of the differential output voltage	$\Delta V_{OD} $	$R_L=100\Omega$ or $R_L=54\Omega$			0.2	
Common-Mode Output Voltage	$ V_{OC} $	$R_L=100\Omega$ or $R_L=54\Omega$		$V_{DD2}/2$	2.8	
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC} $	$R_L=100\Omega$ or $R_L=54\Omega$			0.2	V
Driver Short-Circuit Output Current	$I_{OSD}$	$0 \leq V_{OUT} \leq +12V$			100	mA
		$-7V \leq V_{OUT} \leq V_{DD2}$	-100			
<b>Receiver</b>						
Input Current (A and B)	$I_A, I_B$	DE=GND, $V_{DD2}=GND$ or $V_{DD2}, V_{IN}=12V$			80	uA
		DE=GND, $V_{DD2}=GND$ or $V_{DD2}, V_{IN}=-7V$	-60			
Receiver Differential Threshold Voltage	$V_{TH}$	$-7V \leq V_{CM} \leq 12V$	-200	-125	-50	mV
Receiver Input Hysteresis	$\Delta V_{TH}$	$V_A+V_B=0$		40		mV
Receiver Input Resistance	$R_{IN}$	$-7V \leq V_{CM} \leq 12V, DE=low$	96k $\Omega$			

## 8.2 Switching Electrical Characteristics

$V_{DD1} = 2.5V \sim 5V, V_{DD2} = 2.5V \sim 5.5V, T_A = -40$  to  $85^\circ C$ . Unless otherwise noted, Typical values are at  $V_{DD1} = 5V, V_{DD2} = 5V, T_A = 25^\circ C$  )

**Table 4. Switching Electrical Characteristics**

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Driver</b>						
Maximum Data Rate	$f_{MAX}$				12	Mbps
Driver Propagation Delay	$t_{PLH}$			11.5	50	ns
	$t_{PHL}$			13.2	50	ns
Driver Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	PWD			1	10	ns

Driver Output Falling Time or Rising time	$t_F$			1.7	16	ns
	$t_R$			1.8	16	
Driver Enable to Output High	$t_{ZH}$			30	60	ns
Driver Enable to Output Low	$t_{ZL}$			30	60	ns
Driver Output High to Disable	$t_{HZ}$			18	60	ns
Driver Output Low to Disable	$t_{LZ}$			12	60	ns
<b>Receiver</b>						
Maximum Data Rate	$f_{MAX}$				12	Mbps
Receiver Propagation Delay	$t_{PLH}$	$C_L=15pF$		90	200	ns
	$t_{PHL}$	$C_L=15pF$		75	200	
Receiver Pulse Width Distortion	PWD	$C_L=15pF$		3	20	ns
Receiver Output Falling Time or Rising time	$t_F$	$C_L=15pF$		4.5	6	ns
	$t_R$	$C_L=15pF$		4.5	6	
Receiver Enable to Output High	$t_{ZH}$	$R_L=1k\Omega, C_L=15pF$		30	80	ns
Receiver Enable to Output Low	$t_{ZL}$	$R_L=1k\Omega, C_L=15pF$		30	80	ns
Receiver Disable to Output High	$t_{HZ}$	$R_L=1k\Omega, C_L=15pF$		18	60	ns
Receiver Disable to Output Low	$t_{LZ}$	$R_L=1k\Omega, C_L=15pF$		12	60	ns

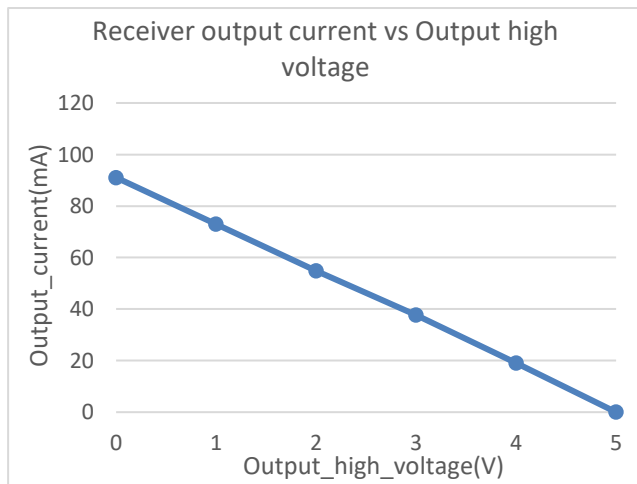
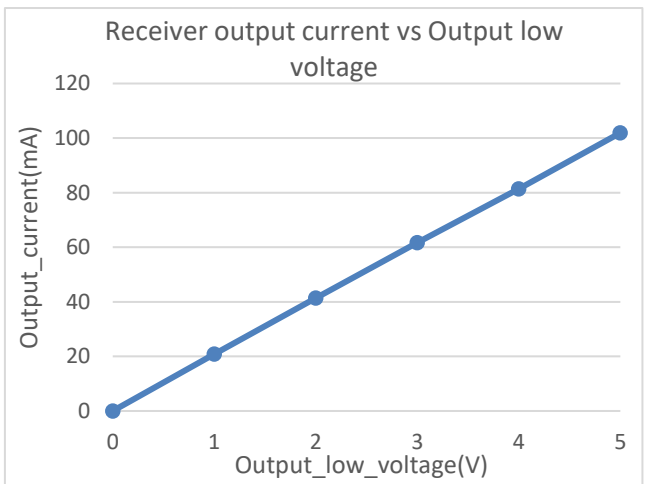
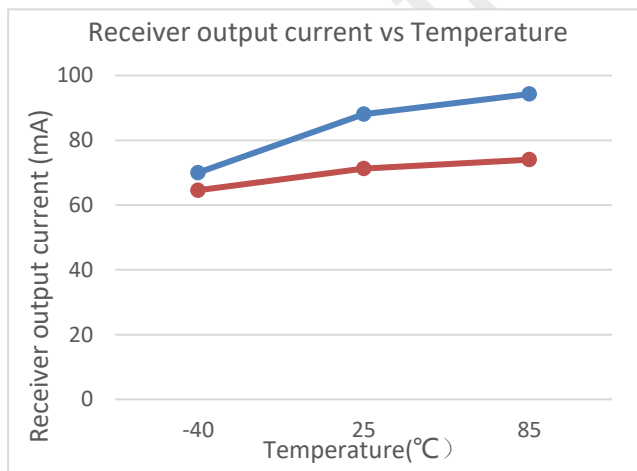
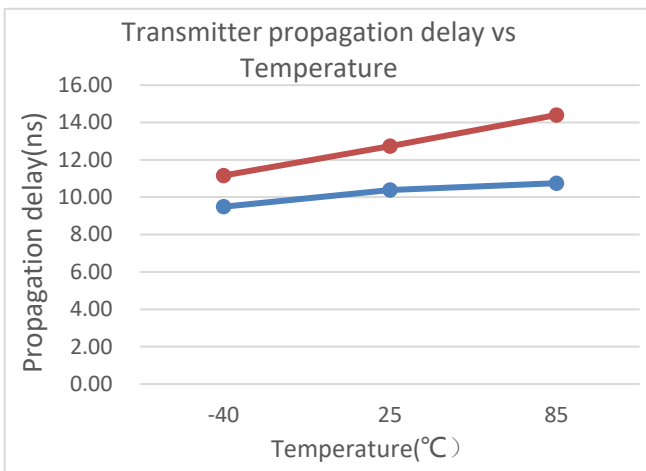
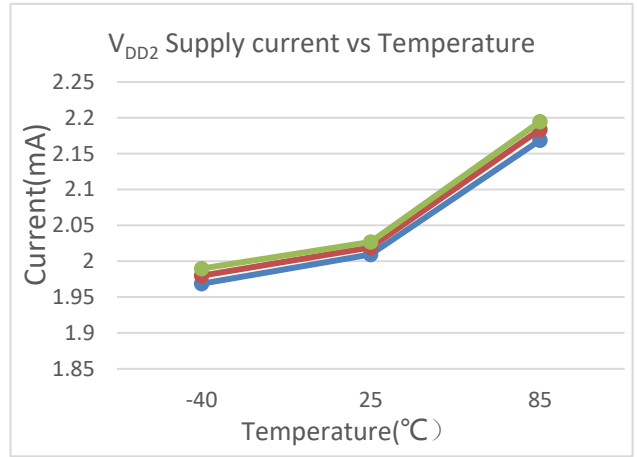
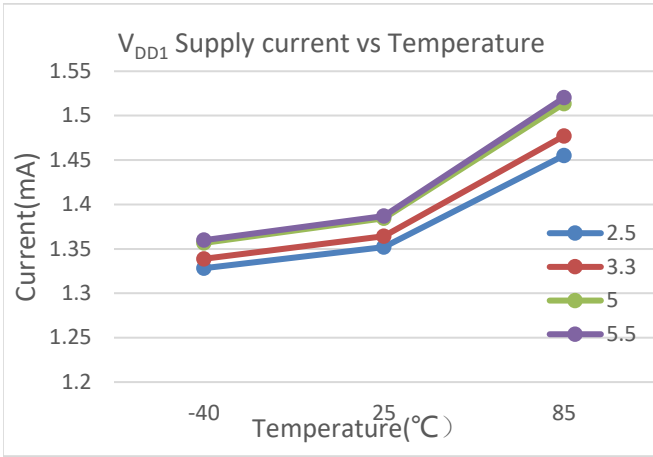
### 8.3 Insulation Specifications

**Table 5. Insulation Specifications**

Parameters	Sym.	Condition	Value	Unit
External clearance <sup>[1]</sup>	CLR	The shortest terminal-to-terminal distance through air	8.0	mm
External creepage <sup>[1]</sup>	CRP	The shortest terminal-to-terminal distance across the package surface	8.0	mm
Distance through insulation	DTI	Minimum internal gap	26	um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
Material group	-		II	-
<b>DIN VDE V 0884-11:2017-01<sup>[2]</sup></b>				
Voltage Classification as standard of IEC 60664-1		For Rated Mains Voltage $\leq 150V_{rms}$	I to IV	
		For Rated Mains Voltage $\leq 300V_{rms}$	I to IV	

		For Rated Mains Voltage $\leq 300V_{rms}$	I to IV	
Pollution Degree per DIN VDE 0110			2	
Maximum repetitive isolation voltage	$V_{IORM}$		1414	$V_{pk}$
Maximum working insulation voltage	$V_{IOWM}$	AC voltage (sine wave); Dielectric layer breakdown (TDDB) test	1000	$V_{RMS}$
		DC voltage	1414	$V_{pk}$
Maximum transient isolation voltage	$V_{IOTM}$	$V_{TEST} = V_{IOTM}$ , $t = 60$ s (certified); $t = 1$ s (100% production)	7000	$V_{pk}$
Maximum surge isolation withstand voltage [3]	$V_{IOSM}$	According to the IEC60065 test, 1.2/50 $\mu$ s waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (certified)	7000	$V_{pk}$
Apparent electric charge [4]	$q_{pd}$	Method a: after the security test subgroup, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd}(m) = 1.2 \times V_{IORM}$ , $t_m = 10$ s	<5	pC
		Method a: after the environmental test subgroup1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd}(m) = 1.6 \times V_{IORM}$ , $t_m = 10$ s	<5	
		Method b1: General test (100% production) and preconditioning (test style) $V_{ini} = V_{IOTM}$ , $t_{ini} = 1$ s; $V_{pd}(m) = 1.875 \times V_{IORM}$ , $t_m = 1$ s	<5	
Insulation capacitance, from input to output <sup>[5]</sup>	$C_{IO}$	$f = 1$ MHz	0.8	pF
Isolation resistor, from input to output <sup>[5]</sup>	$R_{IO}$	$V_{IO} = 500$ V	$>10^9$	$\Omega$
Input capacitance	$C_I$		2	pF
Total power consumption at 25 °C	$P_s$		1499	mW
Secure input, output, or supply current	$I_s$	$\theta_{JA} = 140$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C		mA
Isolation resistance, from input to output <sup>[5]</sup>	$R_{IO}$	$\theta_{JA} = 84$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C	237	$\Omega$
Temperature	$T_s$		150	°C

## 8.4 Typical Performance



## 9 Safety-related Certifications

**Table 6. Safety-related Certifications**

VDE	UL		CQC
DIN VDE V0884-11:2017-01	UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	GB 4943.1-2011
Certificate number: <a href="#">pending</a>	Certificate number: <a href="#">UL-US-2439077-1</a>	Certificate number: <a href="#">UL-CA-2429797-0</a>	Certificate number: <a href="#">pending</a>

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## 10 Function Description

### 10.1 Function Overview

CMT83085/CMT83087 is a high reliability isolated half duplex RS-485 transceiver. Data isolation is achieved using Cmostek integrated capacitive isolation that allows data transmission between the logic side and the Bus side. CMT83085/CMT83087 is safety certified by UL1577 support 5kVRMS insulation withstand voltages.

### 10.2 Data Rate

The data rate of CMT83085/CMT83087 is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

### 10.3 True Fail-safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -50mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage ( $V_A - V_B$ ) is greater than or equal to -50mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

### 10.4 Truth Tables

**Table 7. Driver Function Table<sup>[1]</sup>**

VDD1	VDD2	Input (D)	Enable Input (DE)	Output (OUTx)	
				A	B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

**Table 8. Receiver Function Table**

VDD1	VDD2	Differential Input ( $V_A - V_B$ )	Enable Input (/RE)	Output(R)
PU	PU	$\geq -50\text{mV}$	L/Open	H
PU	PU	$\leq -200\text{mV}$	L/Open	L
PU	PU	OPEN/SHORT	L/Open	H
PU	PU	X	H	Z

PU	PU	IDLE	L	H
PD	PU	X	X	Z
PU	PD	X	X	H
PD	PD	X	X	Z

1. PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

### 10.5 Thermal Shutdown

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (T<sub>J</sub>) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when T<sub>J</sub> falls below +145°C (typ).

## 11 Packaging Information

The packaging information of the CMT83085/CMT83087 SOIC16 is shown in the figures below.

### 11.1 CMT83085/CMT83087 Wide Body SOIC-16 Packaging

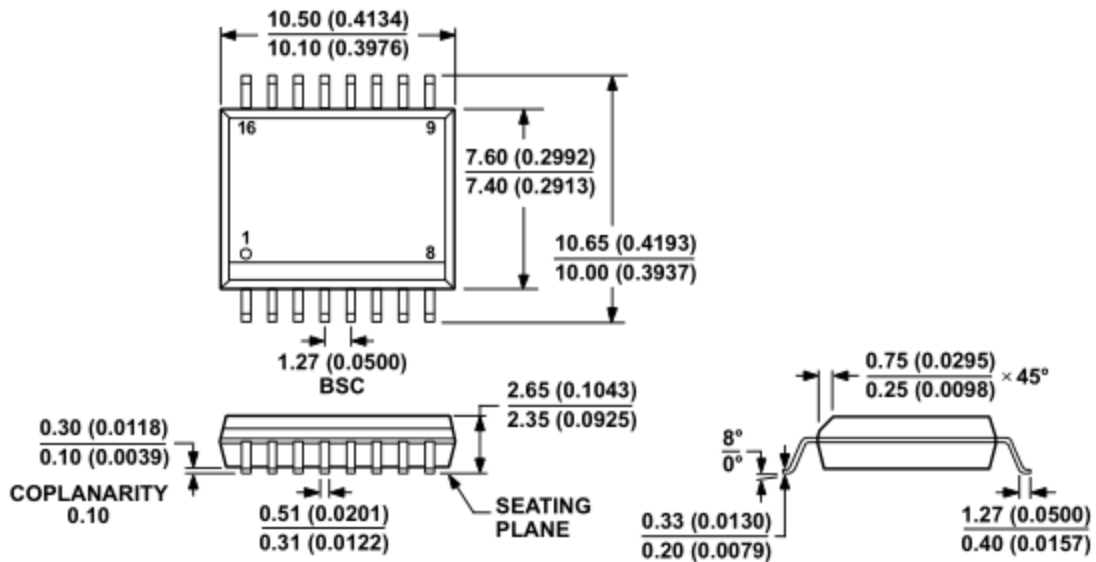


Figure 3. Wide Body SOIC-16 Packaging

Table 2. Wide Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35



Symbol	Scale (mm)		
	Min.	Typ.	Max.
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1	1.40		
$\theta$	0	-	8°

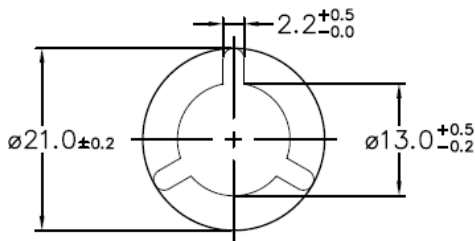
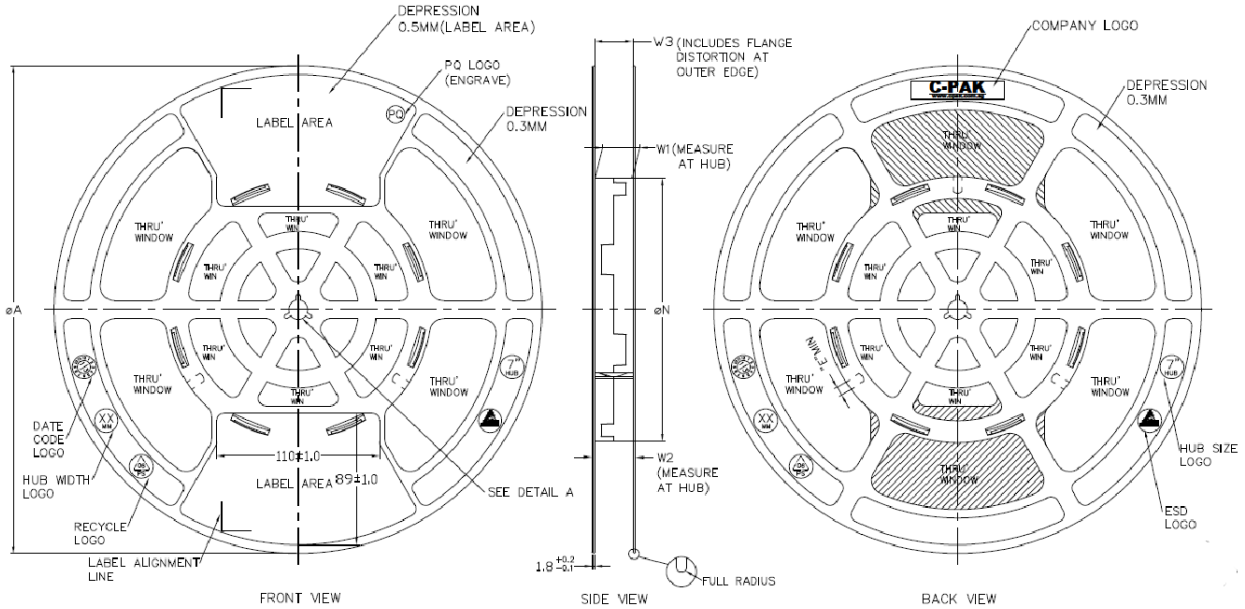
## 12 Ordering Information

**Table 3. Part Number List**

Part Number	MOQ	Isolation Rating (kV)	Duplex	Number of nodes	Max Data Rate (Mbps)	Temperature Range	Package	MSL
CMT83085/ CMT83087	1000	5	Half	256	12	-40 to 125°C	WB SOIC-16	3

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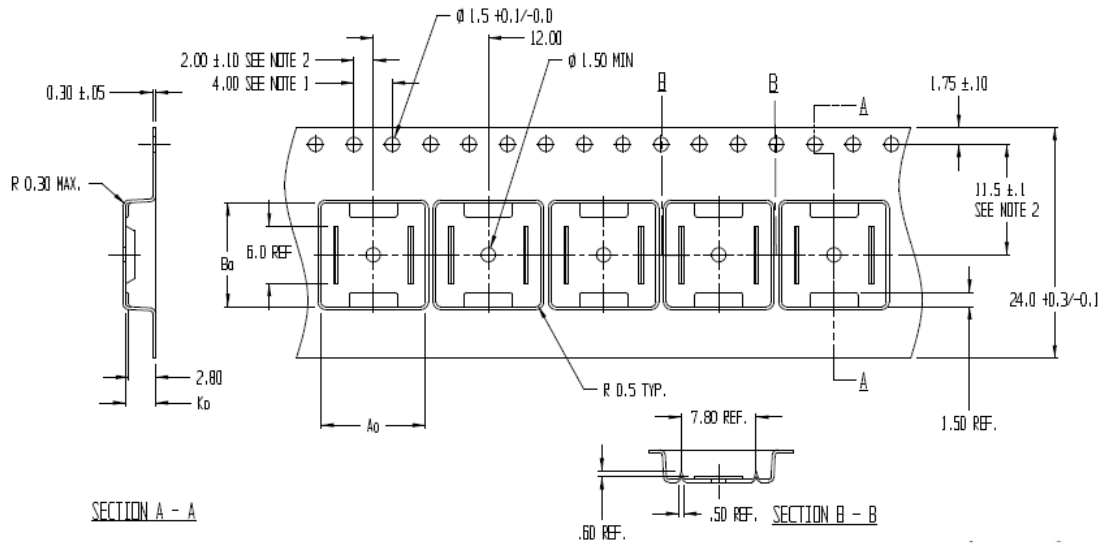
### 13 Tape and Reel Information



ARBOR HOLE  
DETAIL A  
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	∅A ±2.0	∅N ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4		5.5
16MM	330	178	16.4 <sup>+2.0</sup> <sub>-0.0</sub>	22.4		5.5
24MM	330	178	24.4 <sup>+2.0</sup> <sub>-0.0</sub>	30.4		5.5
32MM	330	178	32.4 <sup>+2.0</sup> <sub>-0.0</sub>	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 <sup>12</sup>	ANTISTATIC	ALL TYPES
B	10 <sup>8</sup> TO 10 <sup>11</sup>	STATIC DISSIPATIVE	BLACK ONLY
C	10 <sup>5</sup> & BELOW 10 <sup>5</sup>	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 <sup>9</sup> TO 10 <sup>11</sup>	ANTISTATIC (COATED)	ALL TYPES



NOTES:

1. TO SPROCKET HOLE PITCH CUMULATIVE TOLERANCE  $\pm 0.2$
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3.  $A_0$  AND  $B_0$  ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

$A_0 = 10.90$   
 $B_0 = 10.80$   
 $K_0 = 3.1$

Figure 17. CMT83085/CMT83087 WB SOIC-16 Tape and Reel Information