

ZMCIS373xC General Triple-Channel Digital Isolators

1. Features

- **Data rate: DC to 40Mbps**
- **Robust isolation barrier**
 - High lifetime: >40 years
 - Up to 5000V_{RMS} isolation rating (wide-body package)
 - ±150kV/μs typical CMTI
- **Wide supply range: 3.0V to 5.5V**
- **Wide operating temperature range: -40°C to 125°C**
- **No start-up initialization required**
- **Default output High (ZMCIS373xCH) and Low (ZMCIS373xCL) Options**
- **High electromagnetic immunity**
- **Low power consumption**
 - 2.0mA per channel at 1Mbps with V_{DD} = 5.0V
 - 3.5mA per channel at 40Mbps with V_{DD} = 5.0V
- **Best in class propagation delay and skew**
 - 22ns typical propagation delay
 - 2.5ns propagation delay skew (chip -to-chip)
 - 1ns pulse width distortion
 - 20ns minimum pulse width
- **CMOS inputs logic**
- **Safety regulatory approvals**
 - VDE 0884-17 isolation certification
 - UL according to UL 1577

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated ADC, DAC

3. General Description

The ZM-IS373xC devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS digital I/O. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO₂) insulation barrier, and each channel input integrated Schmitt trigger to provide excellent noise immunity.

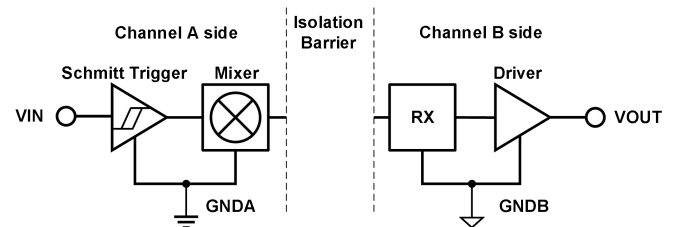
The ZM-IS3730C features 3 channels transferring digital signals in one direction and output enable for the B side is active-high. The ZM-IS3731C device has two forward and one reverse-direction channels, making it ideal for applications such as isolated SPI, RS-485 communication. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H.

The ZM-IS373xC devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin wide-body SOIC package.

Device information

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|---------------|------------------|
| ZMCIS3730C | SOIC16-WB (W) | 10.30mm × 7.50mm |
| ZMCIS3731C | | |

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Table 4- 1 Ordering Guide for Valid Ordering Part Number

| Part Number | Number of Inputs A Side | Number of Inputs B Side | Default Output | Isolation Rating (kV _{RMS}) | Package |
|--------------|----------------------------|----------------------------|----------------|--|---------------|
| ZMCIS3730CLW | 3 | 0 | Low | 5.0 | SOIC16-WB (W) |
| ZMCIS3730CHW | 3 | 0 | High | 5.0 | SOIC16-WB (W) |
| ZMCIS3731CLW | 2 | 1 | Low | 5.0 | SOIC16-WB (W) |
| ZMCIS3731CHW | 2 | 1 | High | 5.0 | SOIC16-WB (W) |

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| 7.8.2 $V_{DDA} = V_{DDB} = 3.3V \pm 10\%$, $T_A = -40$ to 125°C | 9 | 14 | Important Notice | 错误! 未定义书签。 |

5 Revision History

| Revision | Description | Date | Page |
|--------------|-------------|------------|------|
| Version 1.00 | NA | 2024.08.12 | NA |

6 Pin Descriptions and Functions

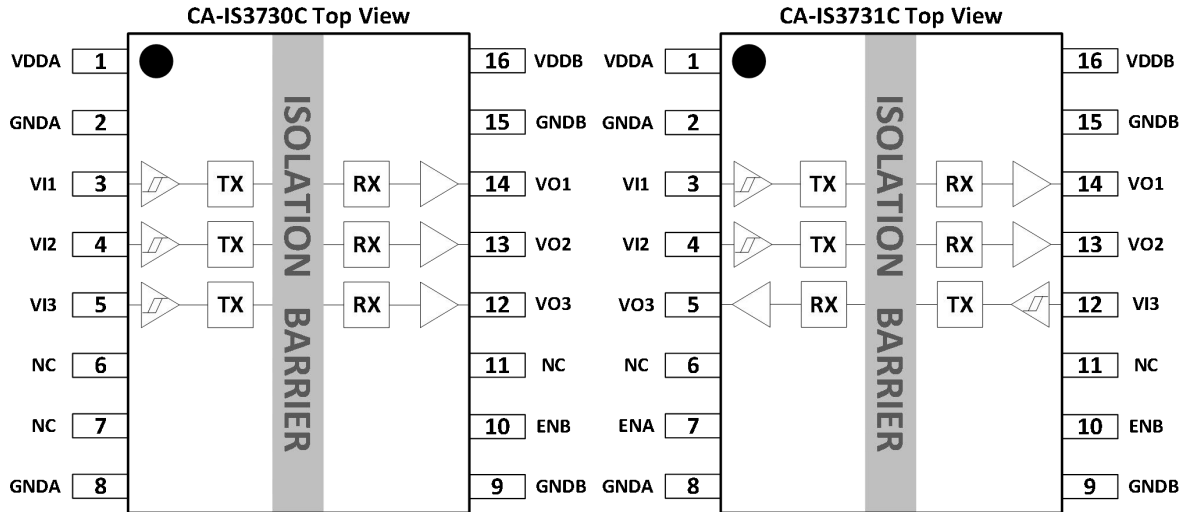


Figure 6- 1. pin configuration

Table 6- 1. Pin description for ZM-IS373xC

| 16-SOIC Pin# | | Name | Type | Description |
|--------------|------------|------------------|-------------|--|
| ZMCIS3730C | ZMCIS3731C | | | |
| 1 | 1 | VDDA | Supply | Power supply for side A. |
| 2, 8 | 2, 8 | GNDA | Ground | Ground reference for side A. |
| 3 | 3 | VI1 | Digital I/O | Digital input 1 on side A, corresponds to logic output 1 on side B. |
| 4 | 4 | VI2 | Digital I/O | Digital input 2 on side A, corresponds to logic output 2 on side B. |
| 5 | 12 | VI3 | Digital I/O | Digital input 3 on side A/B, corresponds to logic output 3 on side B/A. |
| 6, 7 | 6 | NC ¹ | No Connect | Not internally connected. They can be left floating, tied to VDDA or tied to GNDA. |
| - | 7 | ENA ² | Digital I/O | Output enable A. Output pin on side A is enabled when ENA is high or floating; Output pin on side A is open and in high-impedance state when ENA is low. |
| 9, 15 | 9, 15 | GNDB | Ground | Ground reference for side B. |
| 11 | 11 | NC ¹ | No Connect | Not internally connected. They can be left floating, tied to VDDB or tied to GNDB. |
| 10 | 10 | ENB ² | Digital I/O | Output enable B. Output pin on side B is enabled when ENB is high or floating; Output pin on side B is open and in high-impedance state when ENB is low. |
| 12 | 5 | VO3 | Digital I/O | Digital output 3 on side B/A, VO3 is the logic output for the VI3 input on side A/B. |
| 13 | 13 | VO2 | Digital I/O | Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A. |
| 14 | 14 | VO1 | Digital I/O | Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A. |
| 16 | 16 | VDDB | Supply | Power supply for side B. |

Notes:

1. No Connect. These pins are not internally connected. They can be left floating, tied to VDD_ or tied to GND.
2. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.

7 Specifications

7.1 Absolute Maximum Ratings¹

| PARAMETER | MIN | MAX | UNIT |
|---|------|-----|------|
| V _{DDA} , V _{DDB} Supply voltage ² | -0.5 | 7.0 | V |

| | | | | |
|-----------|------------------------------|------|-------------------|----|
| V_{IN} | Voltage at V_{IX} , EN_x | -0.5 | $V_{DD-} + 0.5^3$ | V |
| I_O | Output current | -20 | 20 | mA |
| T_J | Junction Temperature | -40 | 150 | °C |
| T_{STG} | Storage Temperature | -65 | 150 | °C |

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-----------------------------------|---|-------|------|
| V_{ESD} Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pins at same side | ±8 | kV |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | ±2 | |

7.3 Recommended Operating Conditions

| PARAMETER | | MIN | NOM | MAX | UNIT |
|--------------------|---|------------------------|------------|------------------------|------|
| V_{DDA}, V_{DDB} | Supply voltage | 3.0 | 3.3 or 5.0 | 5.5 | V |
| $V_{DD} (UVLO+)$ | V_{DDX} undervoltage-lockout threshold @ rising edge | 2.55 | 2.7 | 2.85 | V |
| $V_{DD} (UVLO-)$ | V_{DDX} undervoltage-lockout threshold @ falling edge | 2.35 | 2.5 | 2.65 | V |
| $V_{HYS} (UVLO)$ | V_{DDX} undervoltage-lockout threshold hysteresis | 150 | 200 | 250 | mV |
| I_{OH} | High-level output current | $V_{DDO}^1 = 5V$ | -4 | | mA |
| | | $V_{DDO}^1 = 3.3V$ | -2 | | |
| I_{OL} | Low-level output current | $V_{DDO}^1 = 5V$ | | 4 | mA |
| | | $V_{DDO}^1 = 3.3V$ | | 2 | |
| V_{IH} | High-level input voltage | $0.7 \times V_{DDI}^2$ | | V_{DDI}^2 | V |
| V_{IL} | Low-level input voltage | 0 | | $0.3 \times V_{DDI}^2$ | V |
| DR | Data rate | 0 | | 40 | Mbps |
| T_A | Ambient temperature | -40 | 27 | 125 | °C |
| T_J | Junction temperature | -40 | | 150 | °C |

NOTE:

1. V_{DDO} = output-side supply V_{DD} .
2. V_{DDI} = input-side supply V_{DD} .

7.4 Thermal Information

| THERMAL METRIC | | PACKAGE | UNIT |
|-----------------|--|---------------|------|
| | | SOIC16-WB (W) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 83.4 | °C/W |

7.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------------|---|-----|-----|-----|------|
| ZMCIS3730C | | | | | | |
| P_D | Maximum Power Dissipation | $V_{DDA} = V_{DDB} = 5.5V$, $C_L = 15pF$, $T_J = 150^\circ C$, | | | NA | mW |
| P_{DA} | Maximum Power Dissipation on Side A | Input a 20-MHz 50% duty cycle square | | | NA | mW |
| P_{DB} | Maximum Power Dissipation on Side B | wave | | | NA | mW |
| ZMCIS3731C | | | | | | |
| P_D | Maximum Power Dissipation | $V_{DDA} = V_{DDB} = 5.5V$, $C_L = 15pF$, $T_J = 150^\circ C$, | | | 100 | mW |
| P_{DA} | Maximum Power Dissipation on Side A | Input a 20-MHz 50% duty cycle square | | | 40 | mW |
| P_{DB} | Maximum Power Dissipation on Side B | wave | | | 60 | mW |

7.6 Insulation Specifications

| PARAMETR | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|--------------------|------------------|
| | | | W | |
| CLR | External clearance ¹ | Shortest terminal-to-terminal distance through air | 8 | mm |
| CPG | External creepage ¹ | Shortest terminal-to-terminal distance across the package surface | 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | 28 | μm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 600V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 1000V _{RMS} | I-III | |
| DIN EN IEC 60747-17 (VDE 0884-17)² | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1414 | V _{PK} |
| V _{IOWM} | Maximum working isolation voltage | AC voltage; Time dependent dielectric breakdown (TDDB) Test | 1000 | V _{RMS} |
| | | DC voltage | 1414 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1s (100% production) | 7070 | V _{PK} |
| V _{IMP} | Maximum impulse voltage | 1.2/50-μs waveform per IEC 62368-1 | 8700 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ³ | V _{IOSM} ≥ 1.3 × V _{IMP} ; Tested in air or oil (qualification test), 1.2/50-μs waveform per IEC 62368-1 | 11312 | V _{PK} |
| Q _{pd} | Apparent charge ⁴ | Method a, After input/output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s | ≤ 5 | pC |
| | | Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s | ≤ 5 | |
| | | Method b1, At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁵ | V _{IO} = 0.4 × sin(2πft), f = 1MHz | ~ 0.5 | pF |
| R _{IO} | Isolation resistance ⁵ | V _{IO} = 500V, T _A = 25°C | > 10 ¹² | Ω |
| | | V _{IO} = 500V, 100°C ≤ T _A ≤ 125°C | > 10 ¹¹ | |
| | | V _{IO} = 500V at T _S = 150°C | > 10 ⁹ | |
| | Pollution degree | | 2 | |
| UL 1577 | | | | |
| V _{ISO} | Maximum withstanding isolation voltage | V _{TEST} = V _{ISO} , t = 60s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1s (100% production) | 5000 | V _{RMS} |
| NOTE: | | | | |
| <ol style="list-style-type: none"> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier. Apparent charge is electrical discharge caused by a partial discharge (pd). All pins on each side of the barrier tied together creating a two-terminal device. | | | | |

7.7 Safety-Related Certifications

| VDE | UL (Pending) |
|--|--|
| Certified according to DIN EN IEC60747-17(VDE 0884-17):2021-10; EN IEC60747-17:2020+AC:2021 | Recognized under UL 1577 Component Recognition Program |
| Reinforced Isolation: V_{IORM} : 1414V _{PK} V_{IOTM} : 7070V _{PK} V_{IOSM} : 11312V _{PK} | Single protection SOIC16-WB: 5000V _{RMS} |
| Certification Number Reinforced Isolation Certificate: 40057278 | Certification Number: |

7.8 Electrical Characteristics

7.8.1 $V_{DDA} = V_{DDB} = 5V \pm 10\%$, $T_A = -40$ to $125^\circ C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|----------------------------------|--|------------------------|-------------------|------------------------|-------------|
| V_{OH} | High-level output voltage | $I_{OH} = -4mA$; See Figure 8- 3 | $V_{DDO}^1 - 0.4$ | $V_{DDO}^1 - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 4mA$; See Figure 8- 3 | | 0.2 | 0.4 | V |
| $V_{IT+(IN)}$ | Logic input high level threshold | | $0.7 \times V_{DDI}^1$ | | | V |
| $V_{IT-(IN)}$ | Logic input low level threshold | | | | $0.3 \times V_{DDI}^1$ | V |
| I_{IH} | High-Level input leakage current | $V_{IH} = V_{DDI}^1$ at VIx or ENx | | | 20 | μA |
| I_{IL} | Low-Level input leakage current | $V_{IL} = 0V$ at VIx or ENx | -20 | | | μA |
| Z_o | Output impedance ² | | | 50 | | Ω |
| CMTI | Common mode transient immunity | $V_I = V_{DDI}^1$ or 0V, $V_{CM} = 1200V$; See Figure 8- 4 | 100 | 150 | | kV/ μs |
| C_i | Input capacitance ³ | $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1MHz$, $V_{DD} = 5V$ | | 2 | | pF |

NOTE:

- V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
- The nominal output impedance of each isolator driver is $50\Omega \pm 40\%$.
- Measured from pin to Ground.

7.8.2 $V_{DDA} = V_{DDB} = 3.3V \pm 10\%$, $T_A = -40$ to $125^\circ C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|----------------------------------|--|------------------------|-------------------|------------------------|-------------|
| V_{OH} | High-level output voltage | $I_{OH} = -2mA$; See Figure 8- 3 | $V_{DDO}^1 - 0.4$ | $V_{DDO}^1 - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 2mA$; See Figure 8- 3 | | 0.2 | 0.4 | V |
| $V_{IT+(IN)}$ | Logic input high level threshold | | $0.7 \times V_{DDI}^1$ | | | V |
| $V_{IT-(IN)}$ | Logic input low level threshold | | | | $0.3 \times V_{DDI}^1$ | V |
| I_{IH} | High-Level input leakage current | $V_{IH} = V_{DDI}^1$ at VIx or ENx | | | 20 | μA |
| I_{IL} | Low-Level input leakage current | $V_{IL} = 0V$ at VIx | -20 | | | μA |
| Z_o | Output impedance ² | | | 50 | | Ω |
| CMTI | Common mode transient immunity | $V_I = V_{DDI}^1$ or 0V, $V_{CM} = 1200V$; See Figure 8- 4 | 100 | 150 | | kV/ μs |
| C_i | Input capacitance ³ | $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1MHz$, $V_{DD} = 3.3V$ | | 2 | | pF |

NOTE:

- V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
- The nominal output impedance of each isolator driver is $50\Omega \pm 40\%$.
- Measured from pin to Ground.

7.9 Supply Current

7.9.1 $V_{DDA} = V_{DDB} = 5V \pm 10\%$, $T_A = -40$ to 125°C

| Parameters | Test conditions | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|----------------|-----------|-----|-----|------|
| ZMCIS3730C | | | | | | |
| Supply Current – Outputs disabled | ENB = 0V; $V_{IN} = 0V$ (ZMCIS3730CL); $V_{IN} = V_{DDA}$ (ZMCIS3730CH) | I_{DDA} | | NA | | mA |
| | | I_{DDB} | | NA | | |
| | ENB = 0V; $V_{IN} = V_{DDA}$ (ZMCIS3730CL); $V_{IN} = 0V$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| Supply Current – DC Signal | ENB = V_{DDB} ; $V_{IN} = 0V$ (ZMCIS3730CL); $V_{IN} = V_{DDA}$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| | ENB = V_{DDB} ; $V_{IN} = V_{DDA}$ (ZMCIS3730CL); $V_{IN} = 0V$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| Supply Current – AC Signal | ENB = V_{DDB} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{pF}$ for Each Channel. | 1Mbps (500kHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| | | 10Mbps (5MHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| | | 40Mbps (20MHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| ZMCIS3731C | | | | | | |
| Supply Current – Outputs disabled | ENA = ENB = 0V; $V_{IN} = 0V$ (ZMCIS3731CL); $V_{IN} = V_{DDI}^1$ (ZMCIS3731CH) | I_{DDA} | | 2.1 | 3.5 | |
| | | I_{DDB} | | 3.0 | 4.8 | |
| | ENA = ENB = 0V; $V_{IN} = V_{DDI}$ (ZMCIS3731CL); $V_{IN} = 0V$ (ZMCIS3731CH) | I_{DDA} | | 4.9 | 7.6 | |
| | | I_{DDB} | | 4.6 | 7.2 | |
| Supply Current – DC Signal | ENA = ENB = V_{DDI} ; $V_{IN} = 0V$ (ZMCIS3731CL); $V_{IN} = V_{DDI}$ (ZMCIS3731CH) | I_{DDA} | | 2.1 | 3.5 | |
| | | I_{DDB} | | 3.0 | 4.8 | |
| | ENA = ENB = V_{DDI} ; $V_{IN} = V_{DDI}$ (ZMCIS3731CL); $V_{IN} = 0V$ (ZMCIS3731CH) | I_{DDA} | | 4.9 | 7.6 | |
| | | I_{DDB} | | 4.6 | 7.2 | |
| Supply Current – AC Signal | ENA = ENB = V_{DDI} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{pF}$ for Each Channel. | 1Mbps (500kHz) | I_{DDA} | | 3.7 | 5.9 |
| | | | I_{DDB} | | 3.9 | 6.1 |
| | | 10Mbps (5MHz) | I_{DDA} | | 4.6 | 7.2 |
| | | | I_{DDB} | | 5.5 | 8.5 |
| | | 40Mbps (20MHz) | I_{DDA} | | 6.6 | 10.2 |
| | | | I_{DDB} | | 9.6 | 14.8 |
| Note: | | | | | | |
| 1. V_{DDI} = Input-side supply V_{DD} . | | | | | | |

7.9.2 $V_{DDA} = V_{DDB} = 3.3V \pm 10\%$, $T_A = -40$ to $125^\circ C$

| Parameters | Test conditions | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|--|----------------|-----------|-----|-----|------|
| ZMCIS3730C | | | | | | |
| Supply Current – Outputs disabled | ENB = 0V; $V_{IN} = 0V$ (ZMCIS3730CL); $V_{IN} = V_{DDA}$ (ZMCIS3730CH) | I_{DDA} | | NA | | mA |
| | | I_{DDB} | | NA | | |
| | ENB = 0V; $V_{IN} = V_{DDA}$ (ZMCIS3730CL); $V_{IN} = 0V$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| Supply Current – DC Signal | ENB = V_{DDB} ; $V_{IN} = 0V$ (ZMCIS3730CL); $V_{IN} = V_{DDA}$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| | ENB = V_{DDB} ; $V_{IN} = V_{DDA}$ (ZMCIS3730CL); $V_{IN} = 0V$ (ZMCIS3730CH) | I_{DDA} | | NA | | |
| | | I_{DDB} | | NA | | |
| Supply Current – AC Signal | ENB = V_{DDB} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15pF$ for Each Channel. | 1Mbps (500kHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| | | 10Mbps (5MHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| | | 40Mbps (20MHz) | I_{DDA} | | NA | |
| | | | I_{DDB} | | NA | |
| ZMCIS3731C | | | | | | |
| Supply Current – Outputs disabled | ENA = ENB = 0V; $V_{IN} = 0V$ (ZMCIS3731CL); $V_{IN} = V_{DDI}^1$ (ZMCIS3731CH) | I_{DDA} | | 2.0 | 3.3 | mA |
| | | I_{DDB} | | 2.9 | 4.7 | |
| | ENA = ENB = 0V; $V_{IN} = V_{DDI}$ (ZMCIS3731CL); $V_{IN} = 0V$ (ZMCIS3731CH) | I_{DDA} | | 4.8 | 7.5 | |
| | | I_{DDB} | | 4.5 | 7.0 | |
| Supply Current – DC Signal | ENA = ENB = V_{DDI} ; $V_{IN} = 0V$ (ZMCIS3731CL); $V_{IN} = V_{DDI}$ (ZMCIS3731CH) | I_{DDA} | | 2.0 | 3.3 | |
| | | I_{DDB} | | 2.9 | 4.7 | |
| | ENA = ENB = V_{DDI} ; $V_{IN} = V_{DDI}$ (ZMCIS3731CL); $V_{IN} = 0V$ (ZMCIS3731CH) | I_{DDA} | | 4.8 | 7.5 | |
| | | I_{DDB} | | 4.5 | 7.0 | |
| Supply Current – AC Signal | ENA = ENB = V_{DDI} ; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15pF$ for Each Channel. | 1Mbps (500kHz) | I_{DDA} | | 3.5 | 5.6 |
| | | | I_{DDB} | | 3.8 | 6.0 |
| | | 10Mbps (5MHz) | I_{DDA} | | 4.2 | 6.6 |
| | | | I_{DDB} | | 4.8 | 7.5 |
| | | 40Mbps (20MHz) | I_{DDA} | | 5.7 | 8.9 |
| | | | I_{DDB} | | 7.7 | 12.0 |
| Note: | | | | | | |
| 1. V_{DDI} = Input-side supply V_{DD} . | | | | | | |

7.10 Timing Characteristics

7.10.1 $V_{DDA} = V_{DDB} = 5V \pm 10\%$, $T_A = -40$ to 125°C

| Parameters | | Test conditions | MIN | TYP | MAX | UNIT | |
|-----------------------|--|-------------------------|-------------|------|------|---------------|----|
| DR | Data Rate | | 0 | | 40 | Mbps | |
| PW_{min} | Minimum Pulse Width | | | | 20.0 | ns | |
| t_{PLH} , t_{PHL} | Propagation Delay Time | See Figure 8- 1 | | 22.0 | 35 | ns | |
| PWD | Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | | | 2.5 | 10 | ns | |
| $t_{sk(o)}$ | Channel-to-Channel Output Skew Time ¹ | Same-direction channels | | 1 | 3 | ns | |
| $t_{sk(pp)}$ | Part-to-Part Output Skew Time ² | | | 1 | 7 | ns | |
| t_r | Output Signal Rise Time | See Figure 8- 1 | | 2.5 | 4.8 | ns | |
| t_f | Output Signal Fall Time | See Figure 8- 1 | | 2.5 | 4.8 | ns | |
| t_{PHZ} | Disable Propagation Delay, High to High Impedance Output | See Figure 8- 2 | | 8 | 12 | ns | |
| t_{PLZ} | Disable Propagation Delay, Low to High Impedance Output | | | 8 | 12 | ns | |
| t_{PZH} | Enable Propagation Delay, High Impedance to High Output | | ZMCIS373xCL | | 10 | 15 | ns |
| | | | ZMCIS373xCH | | 15 | 22 | ns |
| t_{PZL} | Enable Propagation Delay, High Impedance to Low Output | | ZMCIS373xCL | | 10 | 15 | ns |
| | | | ZMCIS373xCH | | 15 | 22 | ns |
| t_{DO} | Default Output Delay Time from Input Power Loss | See Figure 8- 3 | | 10 | 15 | ns | |
| t_{SU} | Start-up Time | | | 25 | 37 | μs | |

Notes:

- $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

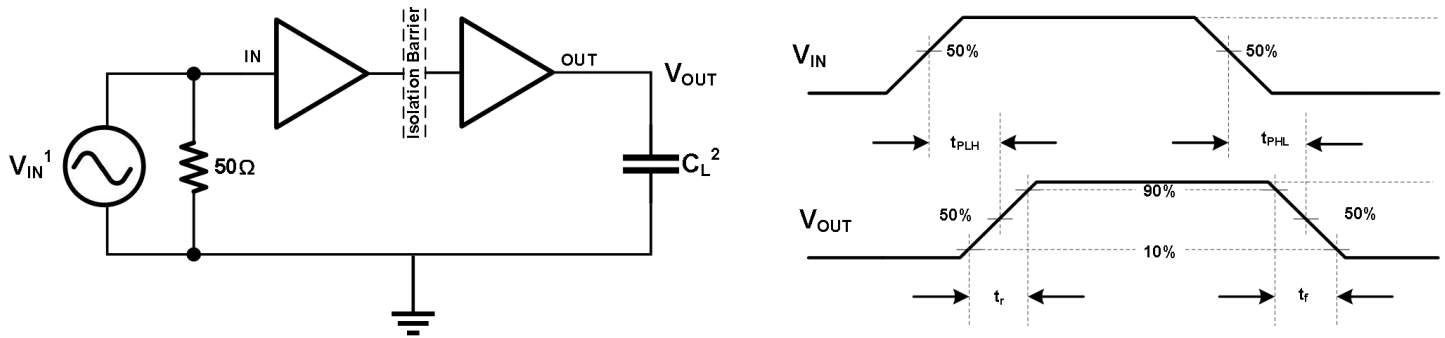
7.10.2 $V_{DDA} = V_{DDB} = 3.3V \pm 10\%$, $T_A = -40$ to 125°C

| Parameters | | Test conditions | MIN | TYP | MAX | UNIT | |
|-----------------------|--|-------------------------|-------------|------|------|---------------|----|
| DR | Data Rate | | 0 | | 40 | Mbps | |
| PW_{min} | Minimum Pulse Width | | | | 20.0 | ns | |
| t_{PLH} , t_{PHL} | Propagation Delay Time | See Figure 8- 1 | | 22.0 | 35 | ns | |
| PWD | Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | | | 2.5 | 10 | ns | |
| $t_{sk(o)}$ | Channel-to-Channel Output Skew Time ¹ | Same-direction channels | | 1 | 3 | ns | |
| $t_{sk(pp)}$ | Part-to-Part Output Skew Time ² | | | 1 | 7 | ns | |
| t_r | Output Signal Rise Time | See Figure 8- 1 | | 2.5 | 4.8 | ns | |
| t_f | Output Signal Fall Time | See Figure 8- 1 | | 2.5 | 4.8 | ns | |
| t_{PHZ} | Disable Propagation Delay, High to High Impedance Output | See Figure 8- 2 | | 8 | 12 | ns | |
| t_{PLZ} | Disable Propagation Delay, Low to High Impedance Output | | | 8 | 12 | ns | |
| t_{PZH} | Enable Propagation Delay, High Impedance to High Output | | ZMCIS373xCL | | 10 | 15 | ns |
| | | | ZMCIS373xCH | | 15 | 22 | ns |
| t_{PZL} | Enable Propagation Delay, High Impedance to Low Output | | ZMCIS373xCL | | 10 | 15 | ns |
| | | | ZMCIS373xCH | | 15 | 22 | ns |
| t_{DO} | Default Output Delay Time from Input Power Loss | See Figure 8- 3 | | 10 | 15 | μs | |
| t_{SU} | Start-up Time | | | 25 | 37 | μs | |

Notes:

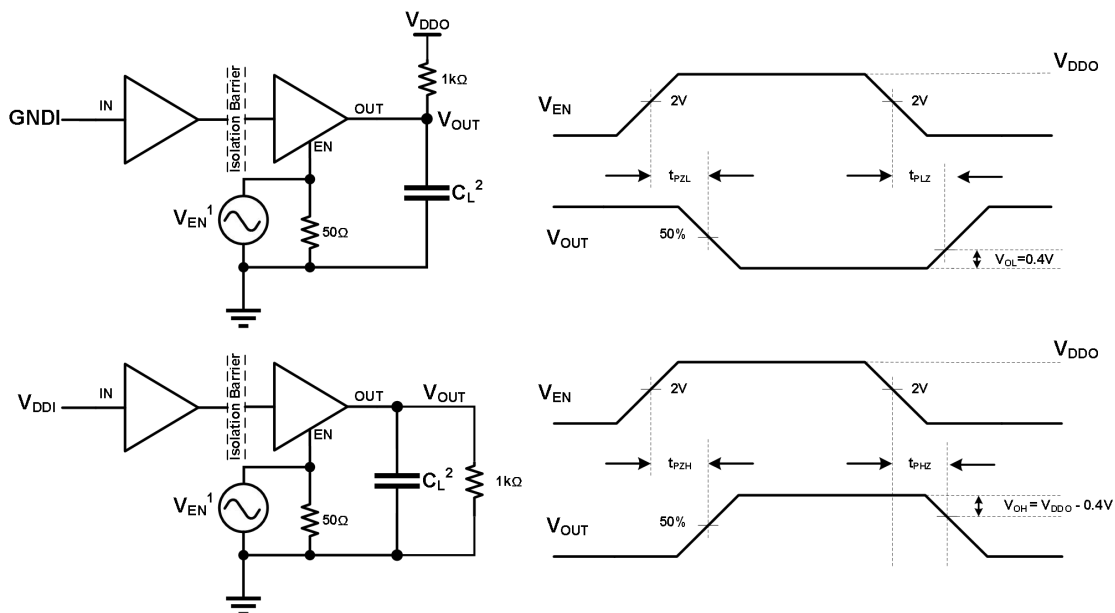
- $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

8 Parameter Measurement Information



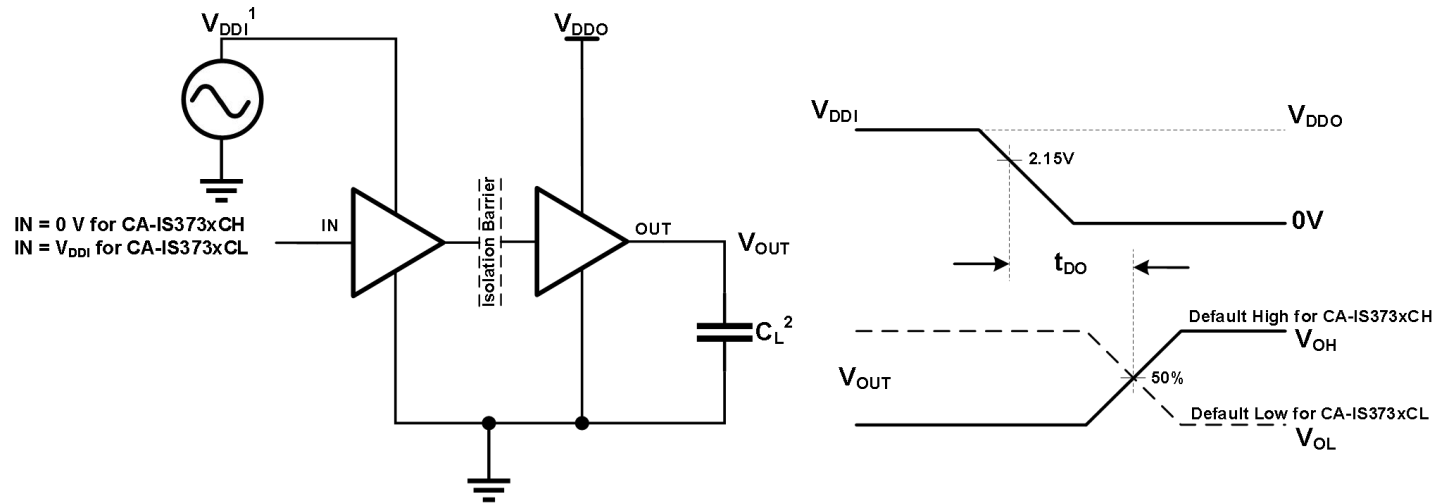
- Note:**
1. A square wave generator provides V_{IN} input signal with characteristics: frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
 2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



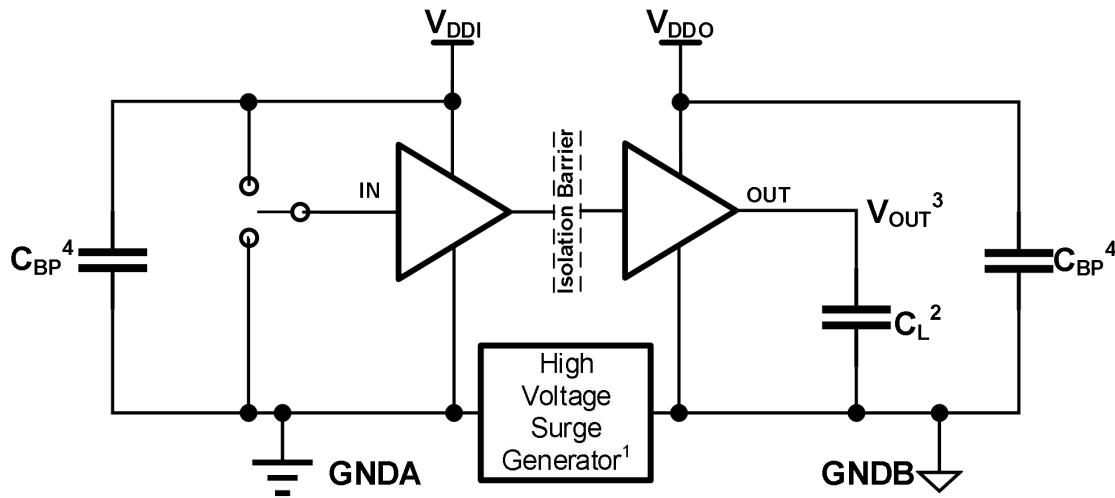
- Note:**
1. A square wave generator provide V_{IN} input signal with characteristics: frequency $\leq 10\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
 2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



- Note:**
1. Power supply ramp rate = 10mV/ns.
 2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

Figure 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms

**Note:**

1. The High Voltage Surge Generator generates repetitive surges with $> 1\text{kV}$, $< 10\text{ns}$ rise time and fall time to reach common-mode transient noise with $> 100\text{kV}/\mu\text{s}$ slew rate.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable whenever the high voltage surges occur.
4. C_{BP} is bypass capacitor, $0.1\mu\text{F} \sim 1\mu\text{F}$.

Figure 8-4. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ZM-IS373xC devices are a family of 3-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovers input signal at output through a buffer stage. With this OOK architecture, the ZM-IS373xC family of devices build a robust data transmission path between different power domains, without any special start-up initialization requirements.

These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 9-1](#), shows a functional block diagram of a typical channel; [Figure 9-2](#) shows the operating waveform of a typical channel.

9.2 Functional Block Diagram

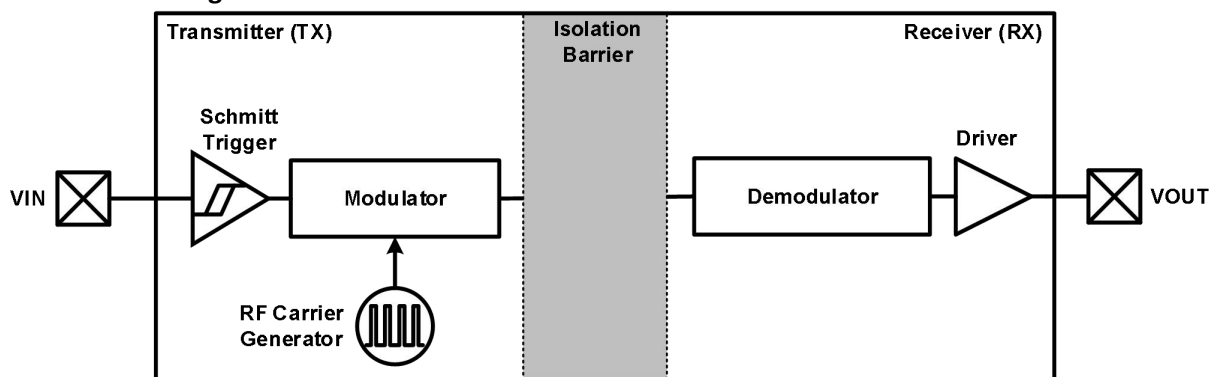


Figure 9- 1 Functional Block Diagram of a Single Channel

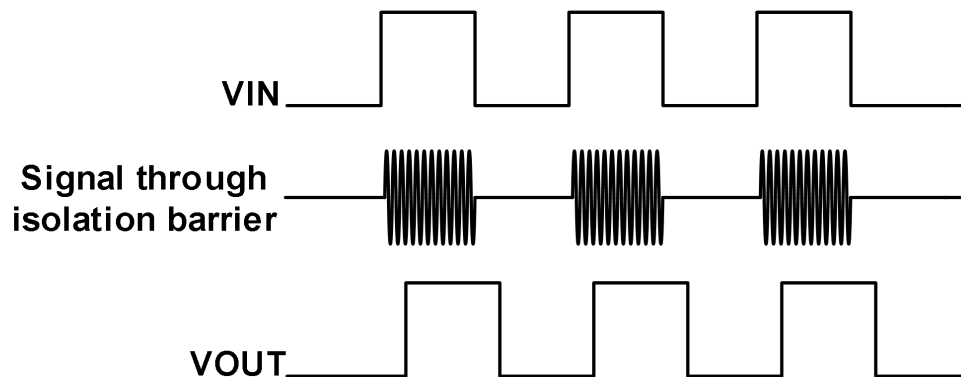


Figure 9- 2 Conceptual Operation Waveform of a Single Channel

9.3 Device Operation Modes

Table 9-1 lists the operation modes for the ZM-IS373xC devices.

Table 9-1 Operation Mode Table¹

| V_{DDI}^1 | V_{DDO}^1 | INPUT (V_{IX}) ² | OUTPUT (V_{OX}) | OPERATION |
|-------------|-------------|---------------------------------|---------------------|---|
| PU | PU | H | H | Normal operation mode: A channel output follows the logic state of the input. |
| | | L | L | |
| | | Open | Default | Default output, fail-safe mode: If a channel input is open, the corresponding channel output goes to the default logic state (Low for ZM-IS373xCL and High for ZM-IS373xCH) |
| PD | PU | X | Default | Default output, fail-safe mode: When V_{DDI}^1 is unpowered, the corresponding channel output goes to the default logic state (Low for ZM-IS373xCL and High for ZM-IS373xCH) |
| X | PD | X | Undetermined | When V_{DDO}^2 is unpowered, the output states are undetermined. ³ |

NOTE:

- V_{DDI} = Input-side Supply V_{DD} ; V_{DDO} = Output-side Supply V_{DD} ; PU = Powered up ($V_{DD_} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD_} \leq V_{DD(UVLO-)}$); X = Irrelevant; H = High level; L = Low level.
- A strongly driven input signal can weakly power the floating V_{DDI} through an internal protection diode and cause undetermined output.
- The outputs are in undetermined state when $V_{DDI} > V_{DD(UVLO+)}$, $V_{DDO} < V_{DD(UVLO-)}$.

Table 9-2 is the truth table with enable input for the ZM-IS373x-Q1 devices.

Table 9-2 Enable Control

| PART NUMBER | ENA ^{1,2} | ENB ^{1,2} | STATUS |
|-------------|--------------------|--------------------|--|
| ZMCIS3730 | — | H | B-side outputs VO1, VO2, VO3 are enabled and each output follows the logic state of its input. |
| | — | L | B-side outputs VO1, VO2, VO3 are disabled, and go to high impedance state. |
| ZMCIS3731 | H | X | A-side output VO3 is enabled and follows the logic state of its input. |
| | L | X | A-side output VO3 is disabled and goes to high impedance state. |
| | X | H | B-side outputs VO1, VO2 are enabled and each output follows the logic state of its input. |
| | X | L | B-side outputs VO1, VO2 are disabled and go to high impedance state. |

NOTE:

- Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.
- X = Irrelevant; H = High level; L = Low level.

10 Application and Implementation

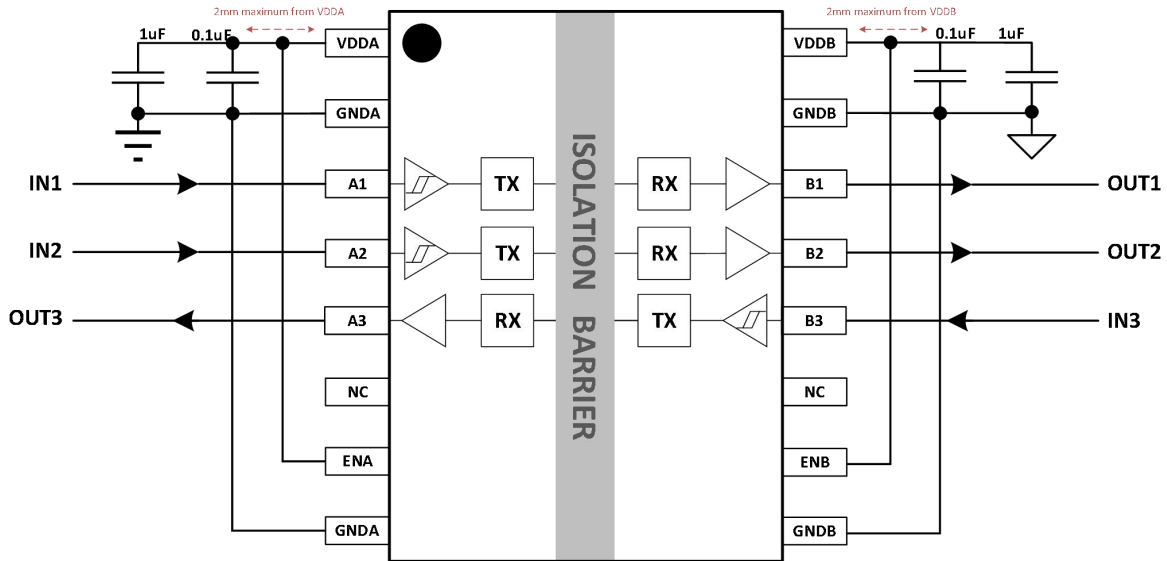


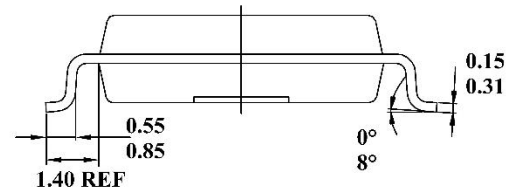
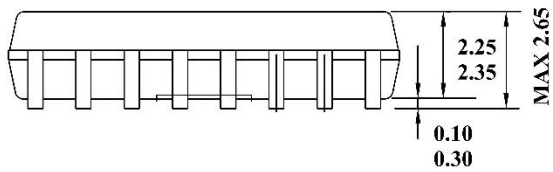
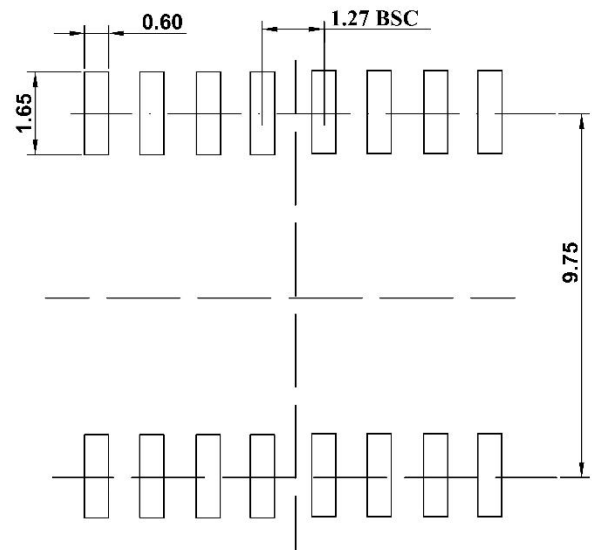
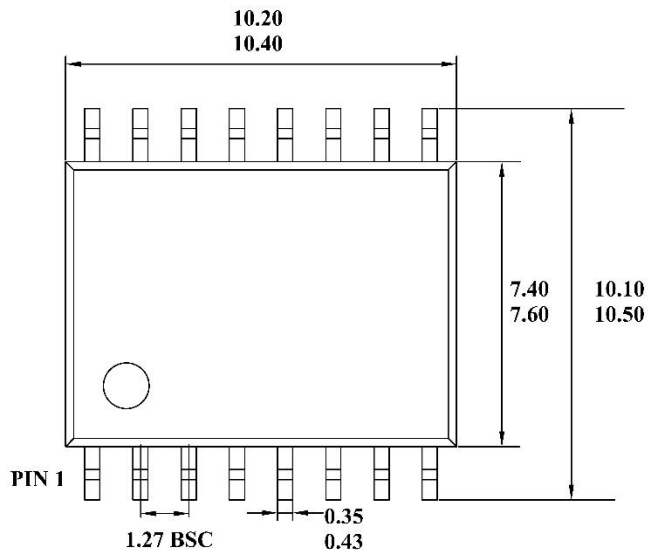
Figure 10- 1 Typical Application Circuit ofZM-IS3731Cx

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, theZM-IS373xC devices only require several external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1 μ F to 1 μ F low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. [Figure 10- 1](#) shows typical operating circuit of theZM-IS373xC devices.

11 Package Information

11.1 SOIC16-WB Package

The values for the dimensions are shown in millimeters.



12 Soldering Information

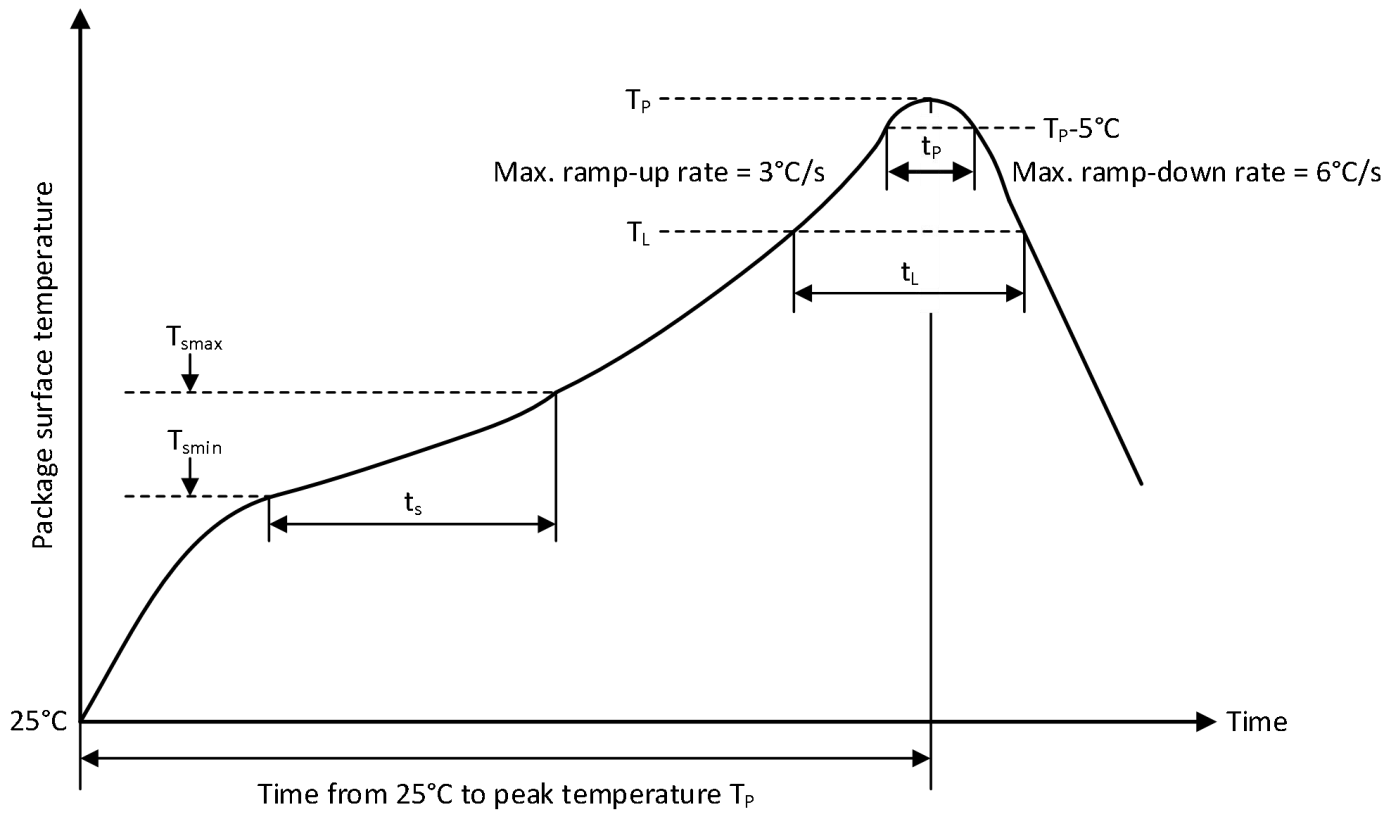


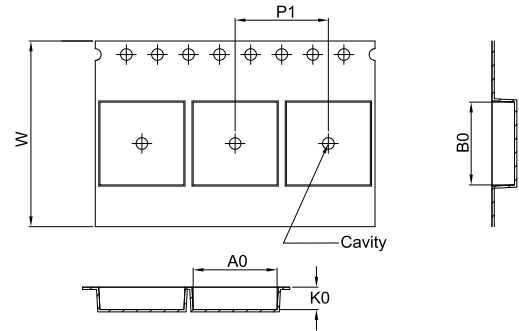
Figure 12- 1 Soldering Temperature Curve

Table 12- 1 Soldering Temperature Parameters

| Profile Feature | Pb-Free Soldering |
|---|-------------------|
| Ramp-up rate ($T_L = 217^\circ\text{C}$ to peak T_P) | 3°C/s max |
| Time t_s of preheat temp ($T_{smin} = 150^\circ\text{C}$ to $T_{smax} = 200^\circ\text{C}$) | 60~120 seconds |
| Time t_L to be maintained above 217°C | 60~150 seconds |
| Peak temperature T_P | 260°C |
| Time t_p within 5°C of actual peak temp | 30 seconds max |
| Ramp-down rate (peak T_P to $T_L = 217^\circ\text{C}$) | 6°C/s max |
| Time from 25°C to peak temperature T_P | 8 minutes max |

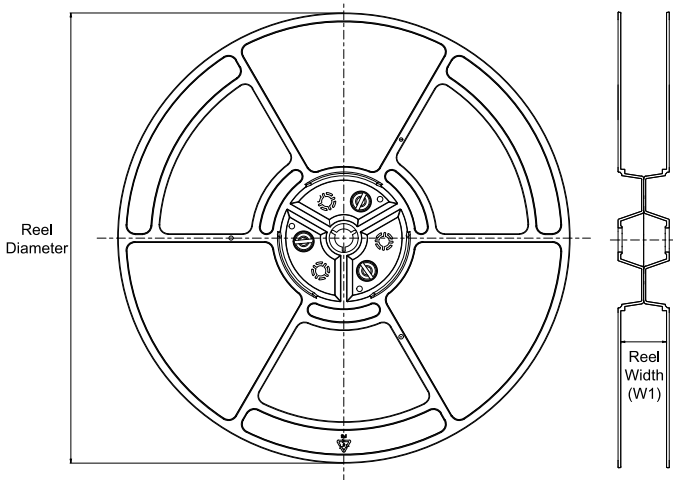
REEL DIMENSIONS

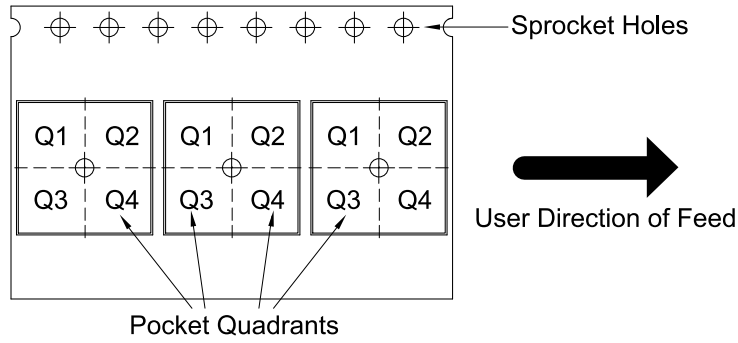
TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE





*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ZMCIS3730CLW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.90 | 10.70 | 3.20 | 12.00 | 16.00 | Q1 |
| ZMCIS3730CHW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.90 | 10.70 | 3.20 | 12.00 | 16.00 | Q1 |
| ZMCIS3731CLW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.90 | 10.70 | 3.20 | 12.00 | 16.00 | Q1 |
| ZMCIS3731CHW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.90 | 10.70 | 3.20 | 12.00 | 16.00 | Q1 |