# 5A, Dual-Channel, High-Speed, Low-Side, Gate-Driver

## Description

The ZMCS5025 device is a dual-channel, high-speed, low-side, gate-driver device capable of effectively driving MOSFET and IGBT power switches. the ZMCS5025 is capable of delivering high-peak current pulses of up to 5A source and 5A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay typically 13ns.

The ZMCS5025 driver feature matched internal propagation delays between the two channels which are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current drive capability or driving two switches in parallel with a single input signal. The input pin thresholds are based on TTL logic, and the input can withstand a maximum supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity

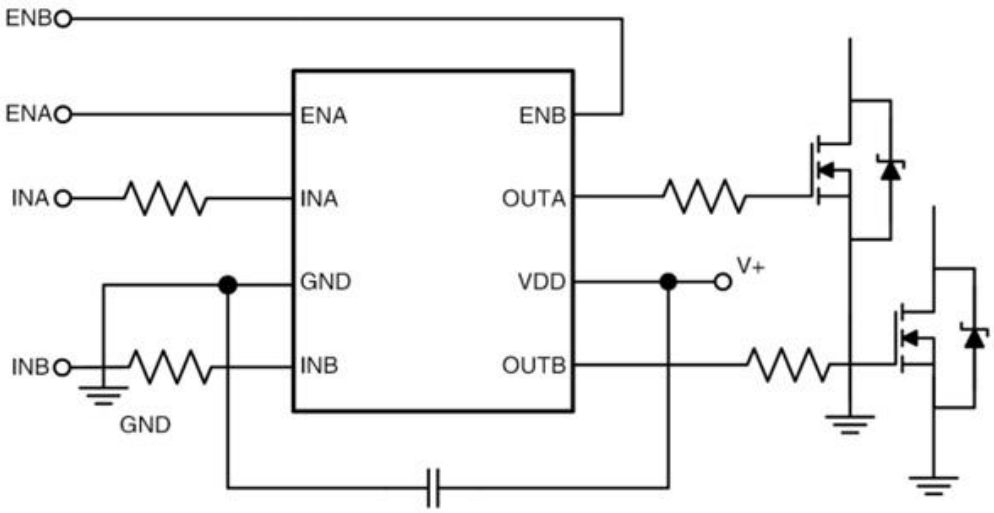
## Applications

- Switch-mode power supplies
- DC-to-DC converters
- Motor control

## Features

- Two independent gate-drive channels
- 5A peak source and sink-drive current
- Independent-enable function for each output
- TTL and CMOS compatible logic threshold independent of supply voltage
- Hysteretic-logic thresholds for high noise immunity
- Inputs and enable pin-voltage levels not restricted by VDD pin bias supply voltage
- 4.5V to 24V single-supply range
- Outputs held low during VDD-UVLO ensures glitch-free operation at power up and power down
- Fast propagation delays (13ns typical)
- Fast rise and fall times
- 1ns typical delay matching between two channels
- Two outputs are paralleled for higher drive current
- Outputs held in low when inputs floating

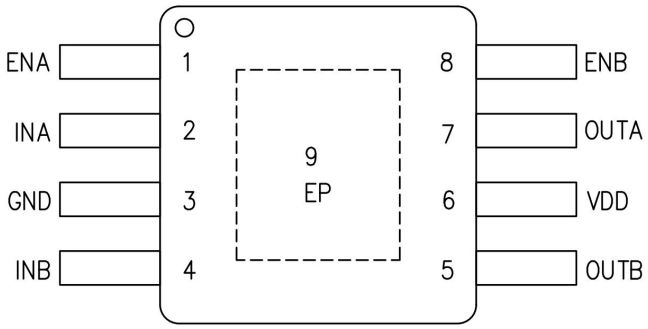
## Typical Application


ENB
ENA
INA
INB
GND
ENA
INA
GND
INB
ENB
OUTA
VDD
OUTB
V+
GND

## Ordering Information

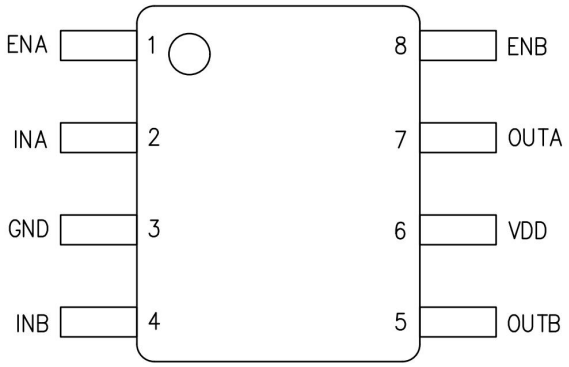
| Tube | Tape and reel | Form factor | Packing |
|---|---|---|---|
| ZMCS5025 | ZMCS5025M | eMSOP8 | Taping/barrel |
| | ZMCS5025S | SOP8 | Taping/barrel |
| | ZMCS5025N | DFN3X3-8L | Taping |

## Pin Functions



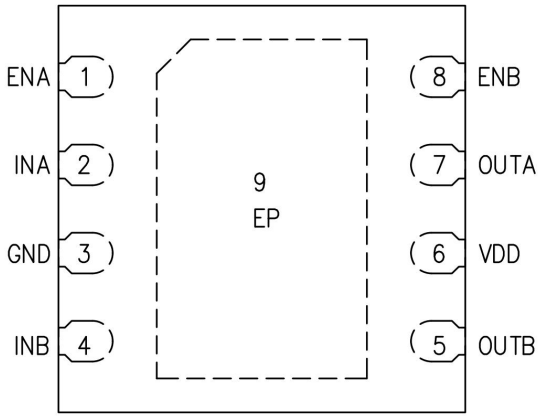

| Pin | Name | Description |
|---|---|---|
| 1 | ENA | Enable input for Channel A |
| 2 | INA | Input to Channel A |
| 3 | GND | Ground |
| 4 | INB | Input to Channel B |
| 5 | OUTB | Output of Channel B |
| 6 | VDD | Supply input |
| 7 | OUTA | Output of Channel A |
| 8 | ENB | Enable input for Channel B |
| 9 | EP | Exposed pad, SOP8 Package None |

## Pin Functions



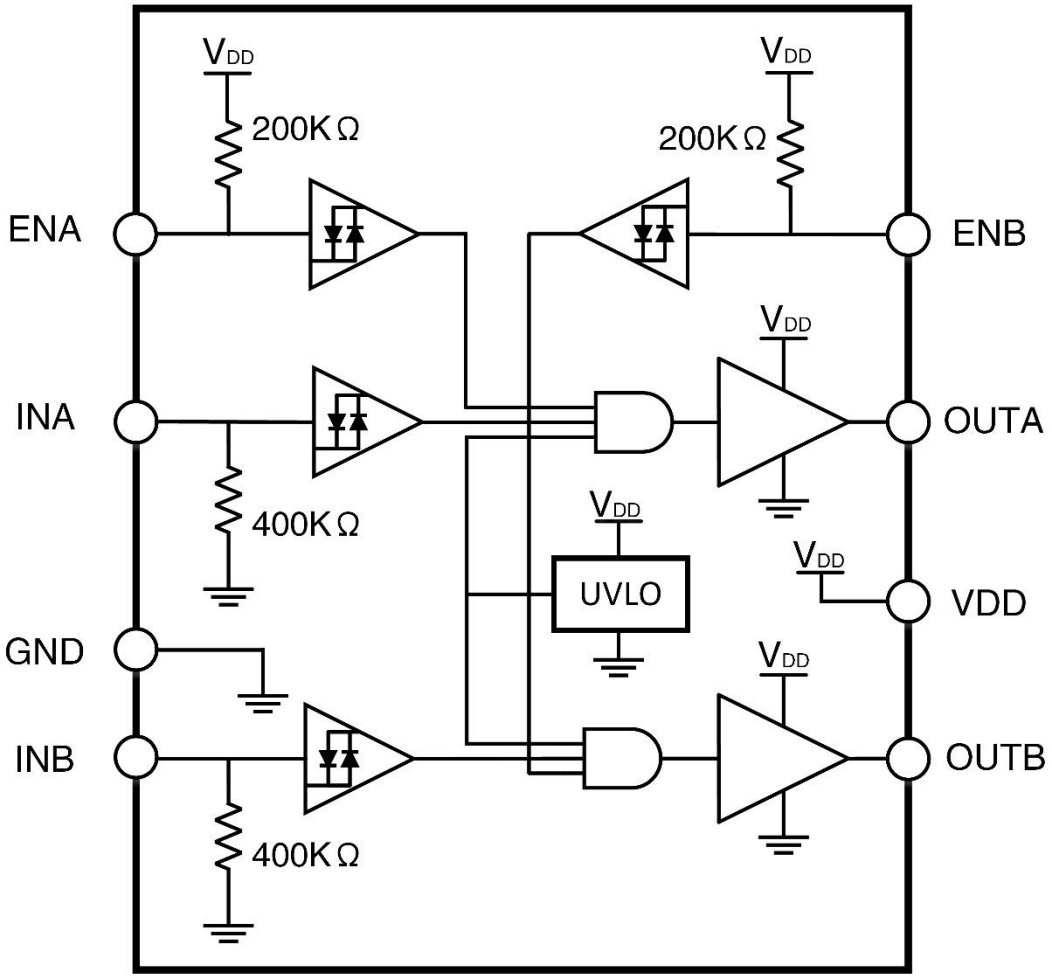

| Pin | Name | Description |
|---|---|---|
| 1 | ENA | Enable input for Channel A |
| 2 | INA | Input to Channel A |
| 3 | GND | Ground |
| 4 | INB | Input to Channel B |
| 5 | OUTB | Output of Channel B |
| 6 | VDD | Supply input |
| 7 | OUTA | Output of Channel A |
| 8 | ENB | Enable input for Channel B |

## Pin Functions




| Pin | Name | Description |
|---|---|---|
| 1 | ENA | Enable input for Channel A |
| 2 | INA | Input to Channel A |
| 3 | GND | Ground |
| 4 | INB | Input to Channel B |
| 5 | OUTB | Output of Channel B |
| 6 | VDD | Supply input |
| 7 | OUTA | Output of Channel A |
| 8 | ENB | Enable input for Channel B |
| 9 | EP | Exposed pad, SOP8 Package None |

## Block Diagram




## Device Logic Table

| ENA | ENB | INA | INB | OUTA | OUTB |
|---|---|---|---|---|---|
| H | H | L | L | L | L |
| H | H | L | H | L | H |
| H | H | H | L | H | L |
| H | H | H | H | H | H |
| L | L | Any | Any | L | L |
| Any | Any | x | x | L | L |
| x | x | L | L | L | L |
| x | x | L | H | L | H |
| x | x | H | L | H | L |
| x | x | H | H | H | H |

## Absolute Maximum Ratings (1)

$V_{DD}$ Voltage.....-0.3V~24V
$V_{OUTA}$ Voltage.....-0.3V~$V_{DD}$+0.3V
$V_{OUTB}$ Voltage.....-0.3V~$V_{DD}$+0.3V
Other pin voltage.....-5V~$V_{DD}$+0.3V
$I_{OUT\_DC}$ current.....0.3A
$I_{OUT\_pulsed}$ current.....5A
Junction Temperature.....150℃
Storage Temperature.....-55℃~+150℃
ESD Rating Human Body Model.....±2KV

(1) Exceeding the maximum operating range can cause permanent damage to the chip. These are stress ratings only and do not imply that the chip functions beyond the specified conditions under these or any other conditions. Working at limit values for long periods of time may affect the reliability of the chip.

## Operating Ratings (1)

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply voltage, VDD | 4.5 | 20 | V |
| Input voltage, INA, INB | 0 | 20 | V |
| Enable voltage, ENA and ENB | 0 | 20 | V |
| Operating Junction Temperature | -40 | 125 | ℃ |

(1) Recommended operating conditions refer to the conditions under which the chip operates normally. For accurate specifications and test conditions, please refer to Electrical Characteristics.

## Dynamic Parameter

Unless otherwise noted, VDD=12V, 1-μF capacitor from VDD to GND, T=25℃。

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| BIAS CURRENTS | | | | | | |
| IDD(off) | Start-up current | $V_{DD}$=3.4V, INA=$V_{DD}$, INB=$V_{DD}$ | 55 | 110 | 175 | uA |
| | | $V_{DD}$=3.4V, INA=GND, INB=GND | 25 | 75 | 145 | |
| UNDERVOLTAGE LOCKOUT (UVLO) | | | | | | |
| VDDON | Supply open threshold | TJ=25℃ | 3.91 | 4.20 | 4.50 | V |
| | | TJ=-55℃~125℃ | 3.70 | 4.20 | 4.65 | |
| VDDOFF | Supply close threshold | | 3.40 | 3.90 | 4.40 | |
| VDD_Hys | Supply voltage hysteresis | | 0.20 | 0.30 | 0.50 | |
| INPUT (INA, INB) | | | | | | |
| VIN_H | Input signal high threshold | | 1.9 | 2.1 | 2.3 | V |
| VIN_L | Input signal low threshold | | 1.0 | 1.2 | 1.4 | |
| VIN_HYS | Input hysteresis | | 0.70 | 0.90 | 1.10 | |
| OUTPUT (OUTA, OUTB) | | | | | | |
| ISNK/ISRC | Peak current (1) | $C_{LOAD}$=0.22μF, $F_{SW}$=1kHz | | ±5 | | A |
| VDD-VOH | High output voltage | $I_{OUT}$=-10mA | | | 0.075 | V |
| VOL | Low output voltage | $I_{OUT}$=10mA | | | 0.01 | |
| ROH | Output pullup resistance | $I_{OUT}$=-10mA | 2.5 | 5 | 7.5 | Ω |
| ROL | Output pulldown resistance | $I_{OUT}$=10mA | 0.15 | 0.5 | 1 | Ω |
| SWITCHING TIME | | | | | | |
| Tr | Rise time | $C_{LOAD}$=1.8nF | | 7 | 18 | ns |
| Tf | Fall time | $C_{LOAD}$=1.8nF | | 6 | 10 | |
| TM | Delay matching between | INA = INB, OUTA and OUTB at 50% transition point | | 1 | 4 | |
| two channels | INA = INB, OUTA and OUTB at 50% transition point | | | 15 | 25 | |
| TPW | Minimum input pulse width that changes the output state | CLOAD=1.8nF, 5-V input pulse | 6 | 13 | 23 | |
| TD1, TD2 | Input to output propagation | CLOAD=1.8nF, 5-V enable pulse | 6 | 13 | 23 | |

(1) Design Assurance.

## Timing Diagrams

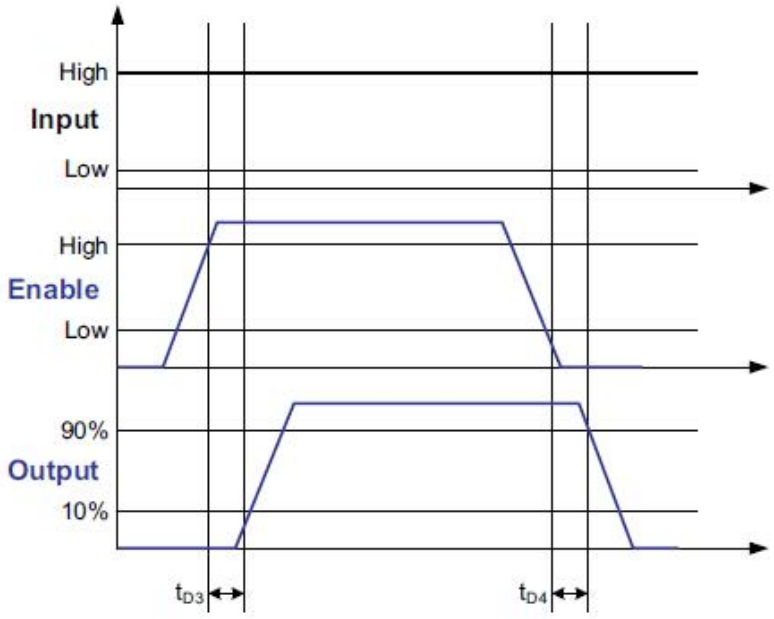



**Figure 1. Enable Function**

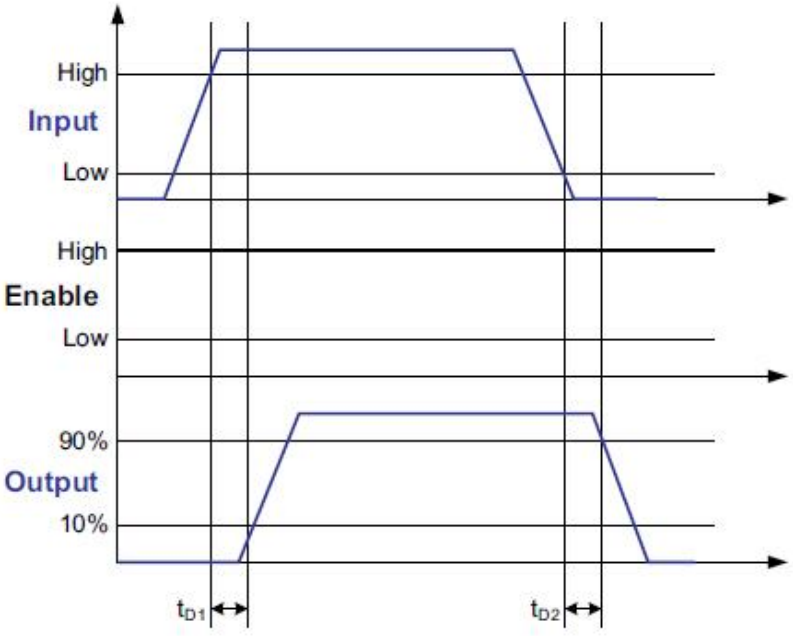


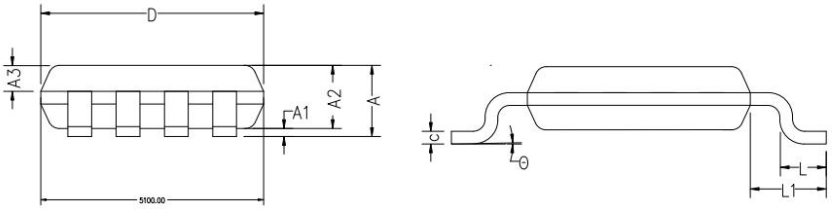

**Figure 2. Input-Output Operation**

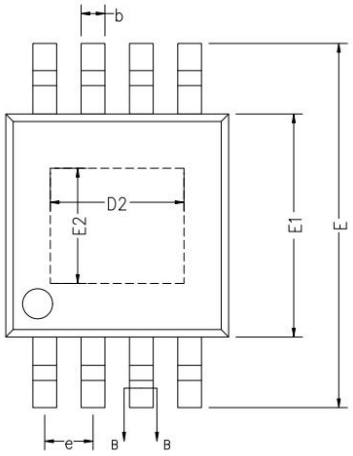
## Application Information

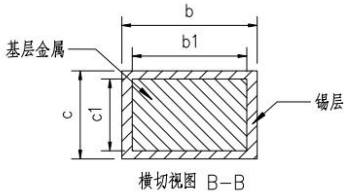
- For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1μF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1μF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The current loop between the load and the capacitor and the current loop between the control signal and the capacitor should be independent of each other, and the two current loops are not allowed to cross.
- In order to ensure the stability of the control signal and the safe operation of the chip, it is recommended to connect a protection resistor in series with each of the input control pins, and the value of the resistor ranges from 50Ω to 200Ω.
- Drive output pull-up current channel should be connected in series with a current limiting resistor, the value of which ranges from 10 ohms to 500 ohms. The pull-down current channel is shorted by a forward diode to the current limiting resistor, which can be omitted if the pull-down speed is not strictly required.
- The ENA pin and ENB pin of the chip contain internal resistors to pull up to VDD, if you don't use this control function, you can leave these two pins empty, and the chip is turned on by default.

## Pod Diagram

eMSOP8



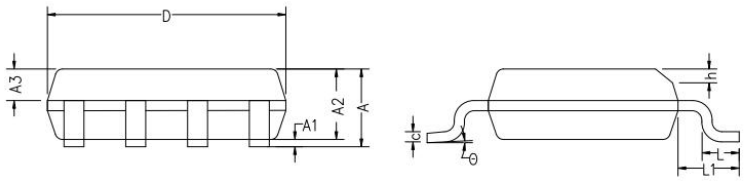



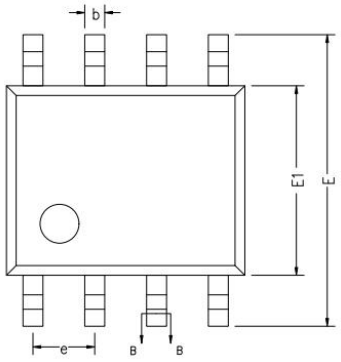



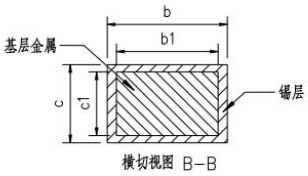

| 符号 | 单位(毫米) | | |
|---|---|---|---|
| | 最小值 | 常规值 | 最大值 |
| A | – | – | 1.10 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| A3 | 0.30 | 0.35 | 0.40 |
| b | 0.28 | – | 0.36 |
| b1 | 0.27 | 0.30 | 0.33 |
| c | 0.15 | – | 0.19 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 理论值0.65 | | |
| L | 0.40 | – | 0.70 |
| L1 | 参考值0.95 | | |
| θ | 0° | – | 8° |
| L/F载体尺寸 (mil) | D2 | E2 | |
| 71*71 | 参考值1.80 | 参考值1.55 | |

## **Pod Diagram**(continued)

SOP8



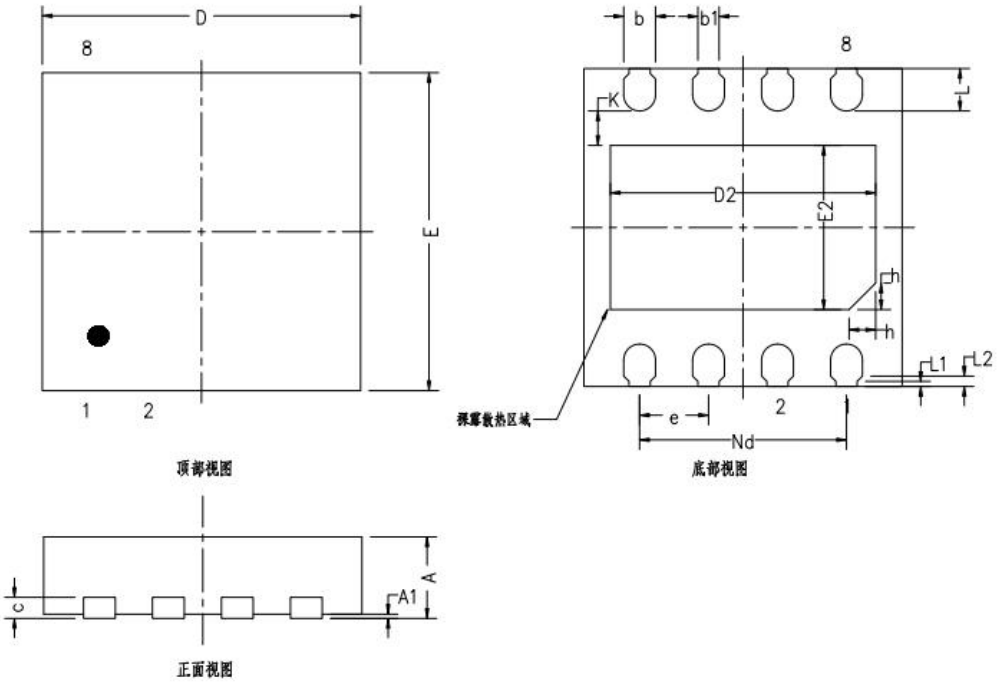




| 符号 | 单位(毫米) | | |
|---|---|---|---|
| | 最小值 | 常规值 | 最大值 |
| A | – | – | 1.750 |
| A1 | 0.100 | – | 0.225 |
| A2 | 1.300 | 1.400 | 1.500 |
| A3 | 0.600 | 0.650 | 0.700 |
| b | 0.390 | – | 0.470 |
| b1 | 0.380 | 0.410 | 0.440 |
| c | 0.200 | – | 0.240 |
| c1 | 0.190 | 0.200 | 0.210 |
| D | 4.800 | 4.900 | 5.000 |
| E | 5.800 | 6.000 | 6.200 |
| E1 | 3.800 | 3.900 | 4.000 |
| e | 理论值1.27 | | |
| h | 0.250 | – | 0.500 |
| L | 0.500 | – | 0.800 |
| L1 | 参考值1.05 | | |
| θ | 0° | – | 8° |

## Pod Diagram(continued)

DFN3*3-8




| 符号 | 单位(毫米) | | |
|---|---|---|---|
| | 最小值 | 常规值 | 最大值 |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.25 | 0.30 | 0.35 |
| b1 | | 参考值0.20 | |
| c | 0.18 | 0.20 | 0.25 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.40 | 2.50 | 2.60 |
| e | | 理论值0.65 | |
| Nd | | 理论值1.95 | |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.45 | 1.55 | 1.65 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | | 参考值0.05 | |
| L2 | | 参考值0.10 | |
| h | 0.20 | 0.25 | 0.30 |
| L/F载体尺寸(mil) | | 106*75 | |