

# Zero-Drift, Rail-to-Rail I/O CMOS Operational Amplifiers

## 1 Features

- **Low Offset Voltage:**  $\pm 1\mu\text{V}$  (TYP)
- **Input Offset Drift:**  $\pm 0.005\mu\text{V}/^\circ\text{C}$
- **High Gain Bandwidth Product:** 4.5MHz
- **Rail-to-Rail Input and Output**
- **High Gain, CMRR, PSRR:** 130dB
- **High Slew Rate:** 2.7V/us
- **Low Noise:** 0.75uVp-p (0.01Hz ~ 10Hz)
- **Low Power Consumption:** 640uA /op amp
- **Overload Recovery Time:** 1us
- **Low Supply Voltage:** +2.7V to +5.5V
- **No External Capacitors Required**
- **Extended Temperature:** -40°C to +125°C

## 2 Applications

- **Temperature Sensors**
- **Medical/ Industrial Instrumentation**
- **Pressure Sensors**
- **Battery-Powered Instrumentation**
- **Active Filtering**
- **Weight Scale Sensor**
- **Strain Gage Amplifiers**
- **Power Converter/ Inverter**

## 3 Description

The ZM8551, ZM8552 and ZM8554 series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (5uV max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offer high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 4.5MHz and slew rate of 2.7V/us.

Single or dual supplies as low as +2.7V ( $\pm 1.35\text{V}$ ) and up to +5.5V ( $\pm 2.75\text{V}$ ) may be used.

The ZM8551/ ZM8552/ ZM8554 are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The ZM8551 single amplifier is available in 5-lead SOT23, 8-lead MSOP and 8-lead SOIC packages, The ZM8552 dual amplifier is available in 8-lead SOIC and 8-lead MSOP narrow surface mount packages, The ZM8554 quad is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
ZM8551	SOT23-5	2.90mm×1.60mm
	SOIC-8 (SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
ZM8552	SOIC-8 (SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
ZM8554	SOIC-14 (SOP14)	8.65mm×3.90mm
	TSSOP-14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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## 4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
C.1	2022/05/17	Initial version completed

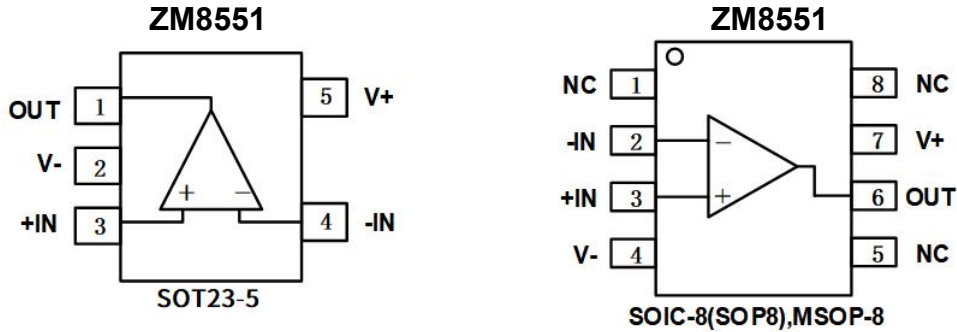
## 5 Package/Ordering Information<sup>(1)</sup>

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking <sup>(2)</sup>	MSL <sup>(3)</sup>	Package Qty
ZM8551XF	SOT23-5	5	1	-40°C ~125°C	8551	MSL3	Tape and Reel,3000
ZM8551XK	SOIC-8 (SOP8)	8	1	-40°C ~125°C	ZM8551	MSL3	Tape and Reel,4000
ZM8551XM	MSOP-8	8	1	-40°C ~125°C	ZM8551	MSL3	Tape and Reel,4000
ZM8552XK	SOIC-8 (SOP8)	8	2	-40°C ~125°C	ZM8552	MSL3	Tape and Reel,4000
ZM8552XM	MSOP-8	8	2	-40°C ~125°C	ZM8552	MSL3	Tape and Reel,4000
ZM8554XP	SOIC-14(SOP14)	14	4	-40°C ~125°C	ZM8554	MSL3	Tape and Reel,4000
ZM8554XQ	TSSOP-14	14	4	-40°C ~125°C	ZM8554	MSL3	Tape and Reel,4000

NOTE:

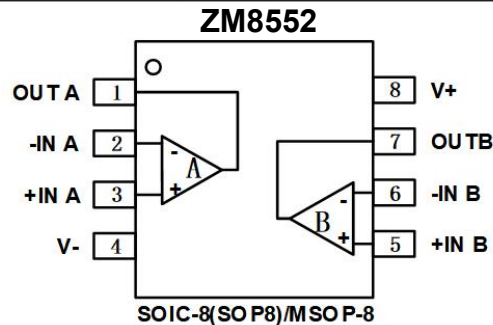
- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) The MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F.

### 6 Pin Configuration and Functions (Top View)



#### Pin Description

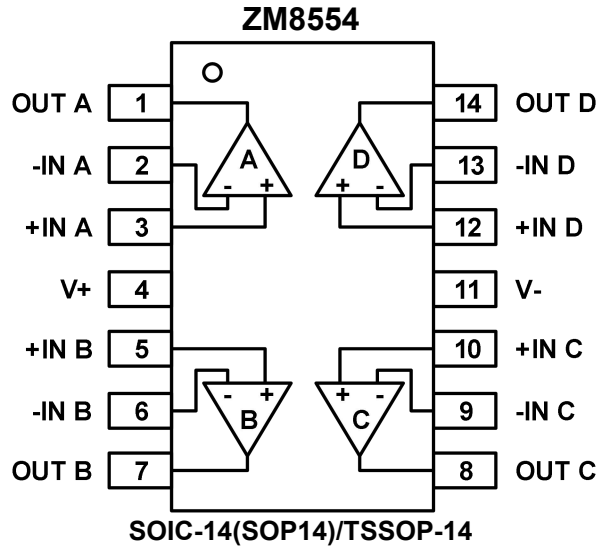
NAME	PIN		I/O	DESCRIPTION
	SOT23-5	SOIC-8 (SOP8)/ MSOP8		
-IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	-	1,5,8	-	No internal connection (can be left floating)
OUT	1	6	O	Output
V-	2	4	-	Negative (lowest) power supply
V+	5	7	-	Positive (highest) power supply



#### Pin Description

NAME	PIN		I/O	DESCRIPTION
	SOIC-8(SOP8) /MSOP-8			
-INA	2		I	Inverting input, channel A
+INA	3		I	Noninverting input, channel A
-INB	6		I	Inverting input, channel B
+INB	5		I	Noninverting input, channel B
OUTA	1		O	Output, channel A
OUTB	7		O	Output, channel B
V-	4		-	Negative (lowest) power supply
V+	8		-	Positive (highest) power supply

Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O	DESCRIPTION
	SOIC-14 (SOP14)/ TSSOP-14		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
Voltage	Supply, $V_S=(V+) - (V-)$		7	V	
	Signal input pin <sup>(2)</sup>	(V-)-0.5	(V+)+0.5		
	Signal output pin <sup>(3)</sup>	(V-)-0.5	(V+)+0.5		
Current	Signal input pin <sup>(2)</sup>	-10	10	mA	
	Signal output pin <sup>(3)</sup>	-55	55	mA	
	Output short-circuit <sup>(4)</sup>	Continuous			
$\theta_{JA}$	Package thermal impedance <sup>(5)</sup>	SOT23-5		230	°C/W
		SOIC-8(SOP8)		110	
		MSOP-8		170	
		SOIC-14(SOP14)		105	
		TSSOP-14		90	
Temperature	Operating range, $T_A$	-40	125	°C	
	Junction, $T_J$	-40	150		
	Storage, $T_{stg}$	-65	150		

(1)Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2)Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(3)Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to  $\pm 50$ mA or less.

(4)Short-circuit to ground, one amplifier per package.

(5)The package thermal impedance is calculated in accordance with JEDEC-51.

(6)The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PCB.

## 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±5000	V
		Machine Model (MM)	±400	



### ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_s = (V+) - (V-)$	Single-supply	2.7		5.5	V
	Dual-supply	±1.35		±2.75	



## 7.4 Electrical Characteristics

Boldface limits apply over the specified temperature range,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

(At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION	ZM8551, ZM8552, ZM8554			
			MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
Input Offset Voltage	$V_{OS}$	$V_{CM} = V_S/2$	-5	$\pm 1$	5	$\mu\text{V}$
Input Offset Voltage Average Drift	$V_{OS} T_C$			$\pm 0.005$	$\pm 0.05$	$\mu\text{V}/^\circ\text{C}$
Power-Supply Rejection Ratio	PSRR	$V_S = +2.7\text{V}$ to $+5.5\text{V}$ , $V_{CM} = 0$	110	130		dB
Channel Separation, dc				0.1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
Input Bias Current	$I_B$	$V_{CM} = V_S/2$		$\pm 50$		pA
Input Offset Current	$I_{OS}$			$\pm 10$		pA
<b>NOISE PERFORMANCE</b>						
Input Voltage Noise	$e_{n,p-p}$	$f = 0.01\text{Hz}$ to $10\text{Hz}$		0.75		$\mu\text{V}_{pp}$
Input Voltage Noise	$e_{n,p-p}$	$f = 0.01\text{Hz}$ to $1\text{Hz}$		0.22		$\mu\text{V}_{pp}$
Input Voltage Noise Density	$e_n$	$f = 1\text{kHz}$		35		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density	$i_n$	$f = 10\text{Hz}$		1.5		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
Common-Mode Voltage Range	$V_{CM}$		(V-) -0.1		(V+) +0.1	V
Common-Mode Rejection Ratio	CMRR	$(V-) -0.1\text{V} < V_{CM} < (V+) + 0.1\text{V}$	110	130		dB
<b>INPUT CAPACITANCE</b>						
Differential				1		pF
Common-Mode				5		pF
<b>OPEN-LOOP GAIN</b>						
Open-Loop Voltage Gain	$A_{OL}$	$R_L = 10\text{k}\Omega$ , $V_O = 0.3\text{V}$ to $4.7\text{V}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	110	130		dB
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$G = +1$		2.7		$\text{V}/\mu\text{s}$
Gain-Bandwidth Product	GBW			4.5		MHz
Overload Recovery Time				1		$\mu\text{s}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{k}\Omega$ to GND	4.99	4.998		V
		$R_L = 10\text{k}\Omega$ to GND	4.95	4.98		V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{k}\Omega$ to V+		1	10	mV
		$R_L = 10\text{k}\Omega$ to V+		10	30	mV
Short-Circuit Current	$I_{SC}$			50		mA
<b>POWER SUPPLY</b>						
Operating Voltage Range	$V_S$		2.7		5.5	V
Quiescent Current/ Amplifier	$I_Q$			640	870	$\mu\text{A}$

### 7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.

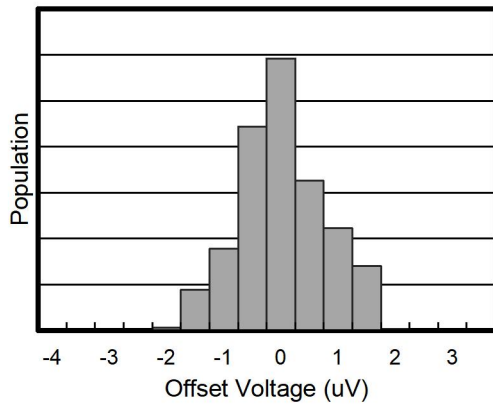


Figure 1. Offset Voltage Production Distribution

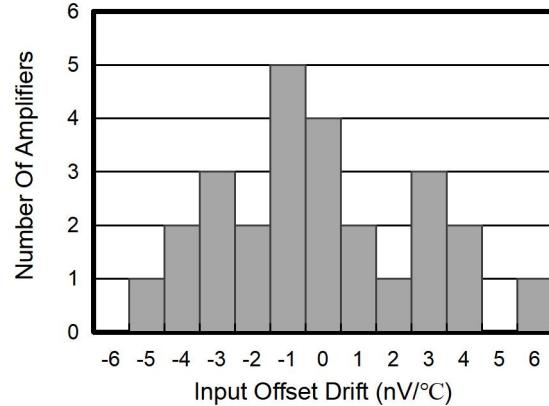


Figure 2. Offset Voltage Drift Production Distribution

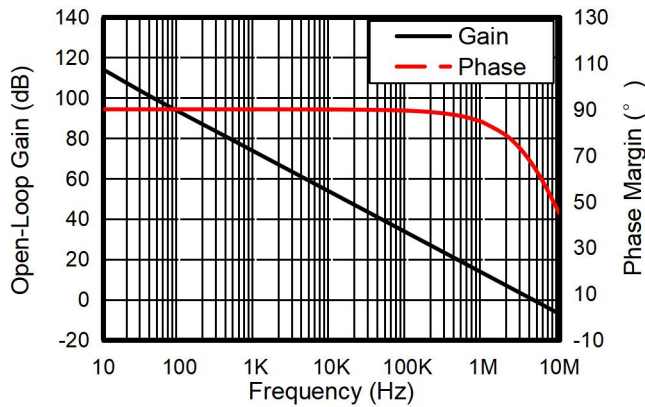


Figure 3. Open-Loop Gain and Phase vs Frequency

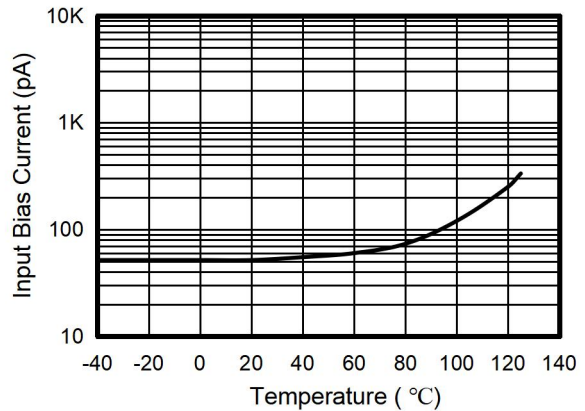


Figure 4. Input Bias Current vs Temperature

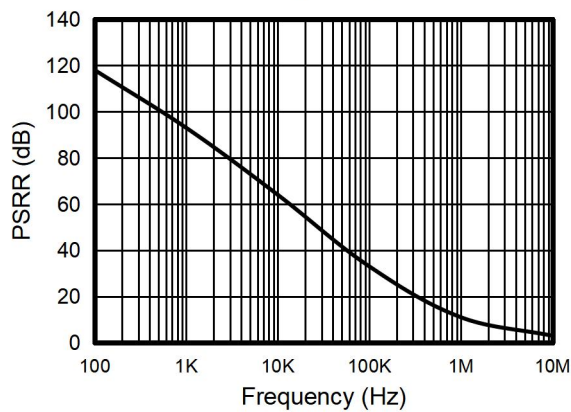


Figure 5. Power-Supply Rejection Ratio vs Frequency

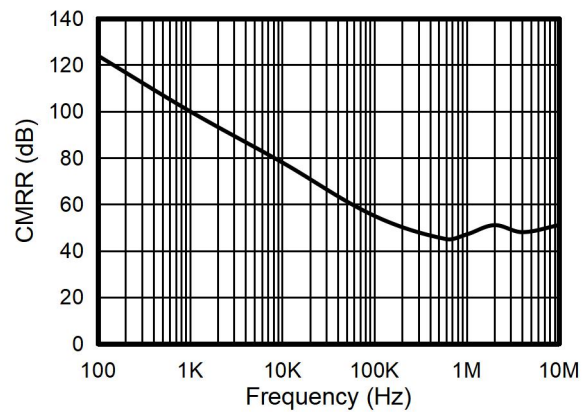
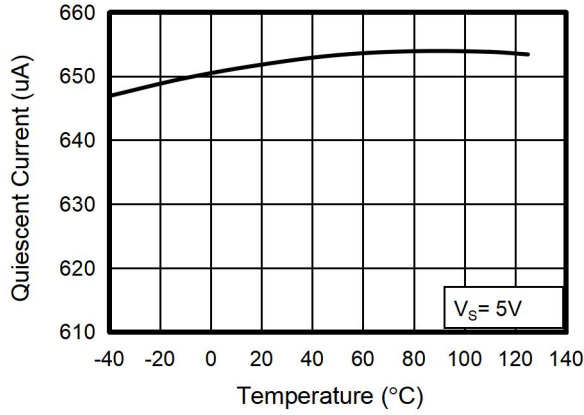


Figure 6. Common-Mode Rejection Ratio vs Frequency

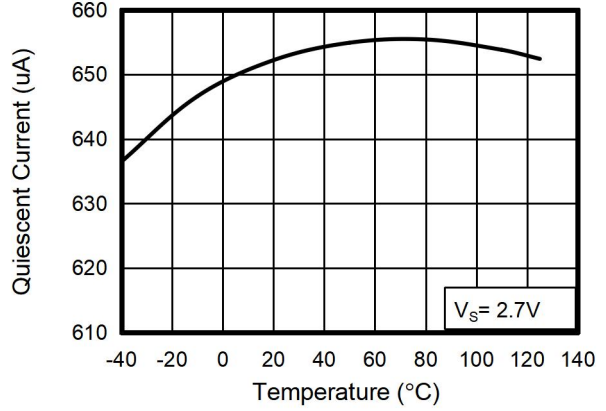
**Typical Characteristics**

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

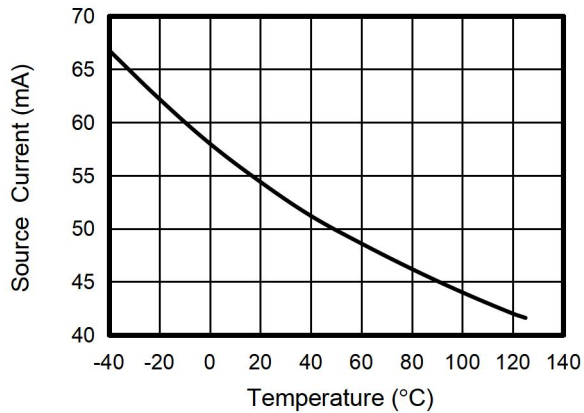
At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.



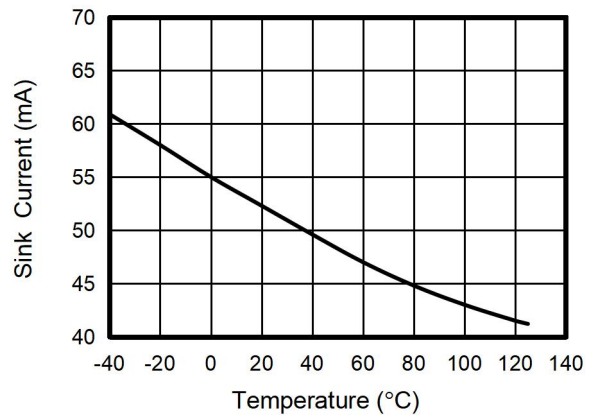
**Figure 7. Quiescent Current vs Temperature**



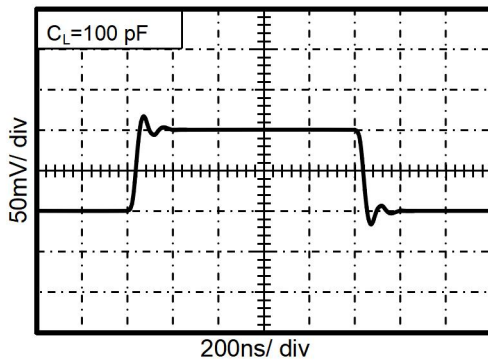
**Figure 8. Quiescent Current vs Temperature**



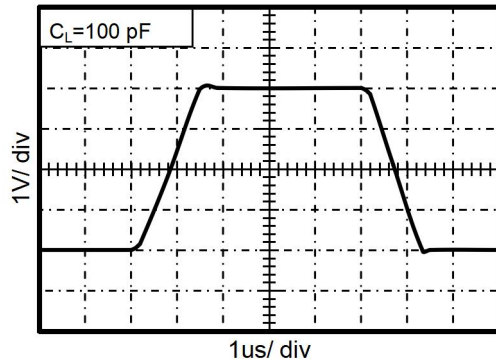
**Figure 9. Source Current vs Temperature**



**Figure 10. Sink Current vs Temperature**



**Figure 11. Small-Signal Step Response**



**Figure 12. Large-Signal Step Response**

### Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.

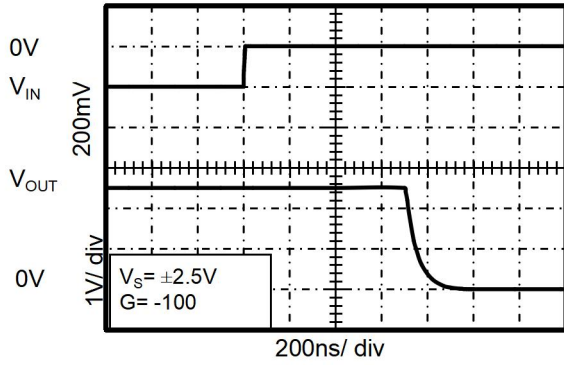


Figure 13. Positive Overvoltage Recovery

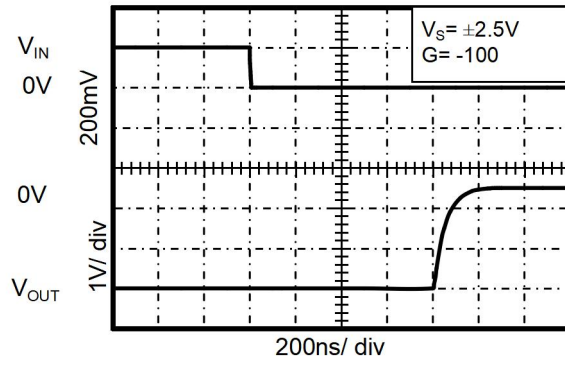


Figure 14. Negative Overvoltage Recovery

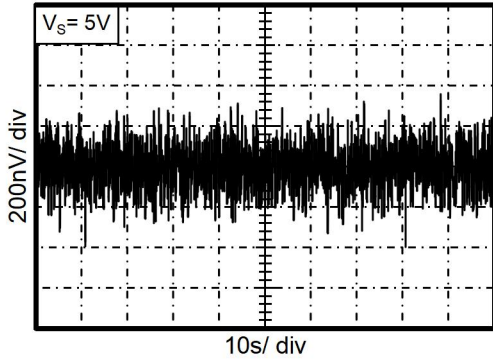


Figure 15. 0.01Hz to 10Hz Noise

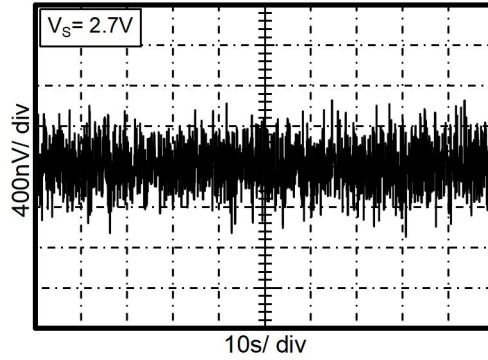


Figure 16. 0.01Hz to 10Hz Noise

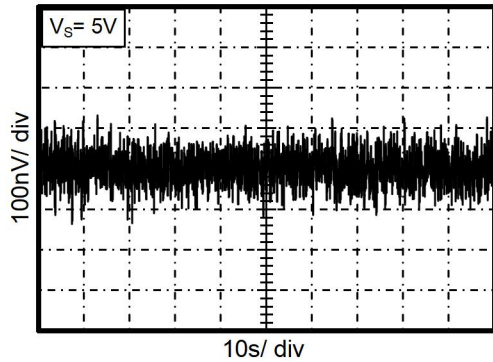


Figure 17. 0.01Hz to 1Hz Noise

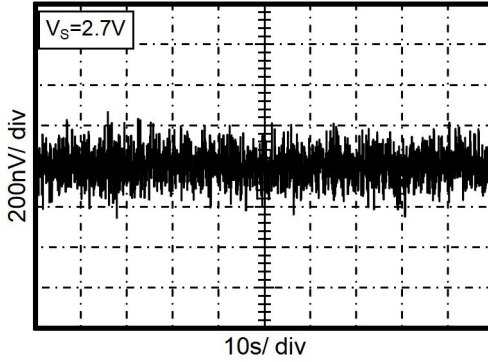


Figure 18. 0.01Hz to 1Hz Noise

## 8 Detailed Description

### 8.1 Overview

The ZM8551, ZM8552, ZM8554 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1 $\mu$ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 $\mu$ V/ $^{\circ}$ C or higher, depending on materials used.

### 8.2 Operating Volatage

The ZM8551, ZM8552, ZM8554 series op amps operate over a power-supply range of +2.7V to +5.5V ( $\pm$ 1.35V to  $\pm$ 2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

## 9 Application Note

The ZM855X is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-uF capacitors are adequate.

### Typical Applications

#### 9.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from -1A to 1A. The single-ended output spans from 110mV to 3.19V. This design uses the ZM855X because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other provides the reference voltage.

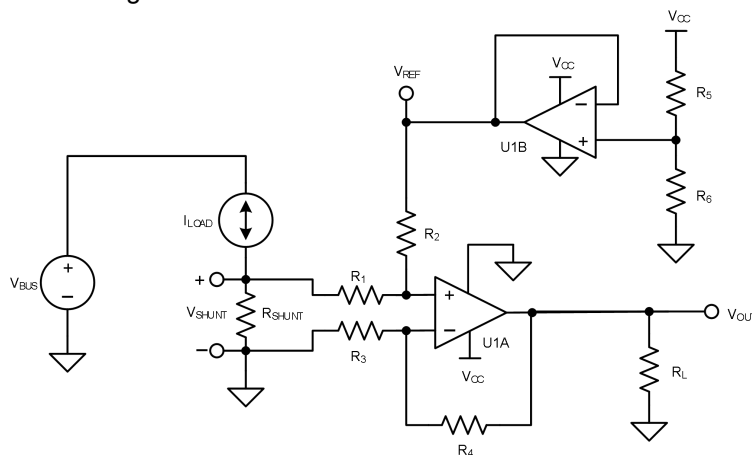


Figure 19. Bidirectional Current-Sensing Schematic

#### 9.2 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: -1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

#### 9.3 Detailed Design Procedure

The load current,  $I_{LOAD}$ , flows through the shunt resistor ( $R_{SHUNT}$ ) to develop the shunt voltage,  $V_{SHUNT}$ . The shunt voltage is then amplified by the difference amplifier, which consists of U1A and  $R_1$  through  $R_4$ . The gain of the difference amplifier is set by the ratio of  $R_4$  to  $R_3$ . To minimize errors, set  $R_2 = R_4$  and  $R_1 = R_3$ . The reference voltage,  $V_{REF}$ , is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times \text{Gain}_{\text{Diff\_Amp}} + V_{REF}$$

Where

$$V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$$

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{R_4}{R_3}$$

$$V_{REF} = V_{CC} \times \left( \frac{R_6}{R_5 + R_6} \right)$$

(1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of  $R_4$  to  $R_3$  and, similarly,  $R_2$  to  $R_1$ . Offset errors are introduced by the voltage divider ( $R_5$  and  $R_6$ ) and how closely the ratio of  $R_4/R_3$  matches  $R_2/R_1$ . The latter value impacts the CMRR of the difference amplifier, which ultimately translates to an offset error. Because this is a low-side measurement, the value of  $V_{SHUNT}$  is the ground potential for the system load. Therefore, it is important to place a maximum

value on  $V_{SHUNT}$ . In this design, the maximum value for  $V_{SHUNT}$  is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \tag{2}$$

### 9.4 Application Note

The tolerance of  $R_{SHUNT}$  is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is -100 mV to 100 mV. This voltage is divided down by  $R_1$  and  $R_2$  before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, it is important to use an operational amplifier, such as the ZM855X, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the ZM855X has a typical offset voltage of  $\pm 1\mu\text{V}$  ( $\pm 5\mu\text{V}$  maximum). Given a symmetric load current of -1 A to 1 A, the voltage divider resistors ( $R_5$  and  $R_6$ ) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10k $\Omega$  resistors were used. To set the gain of the difference amplifier, the common-mode range and output swing of the ZM855X must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the ZM855X given a 3.3V supply.

$$-100\text{mV} < V_{CM} < 3.4\text{V} \tag{3}$$

$$100\text{mV} < V_{OUT} < 3.2\text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2 \text{ V} - 100 \text{ mV}}{100 \text{ m}\Omega \times [1 \text{ A} - (-1\text{A})]} = 15.5 \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for  $R_1$  and  $R_3$  was 1k $\Omega$ . 15.4k $\Omega$  was selected for  $R_2$  and  $R_4$  because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on  $R_1$  through  $R_4$ . As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

### 9.5 Application Curve

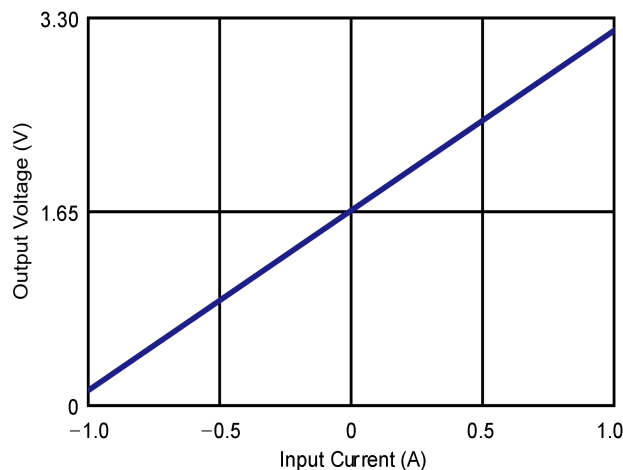


Figure 20. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

## 10 Layout

### 10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

### 10.2 Layout Example

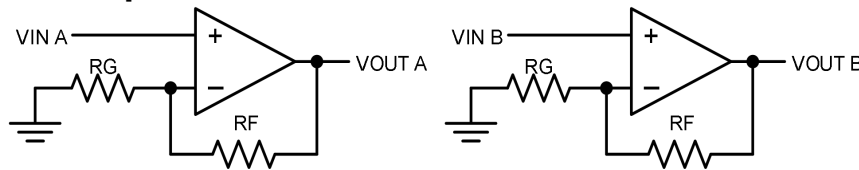


Figure 21. Schematic Representation

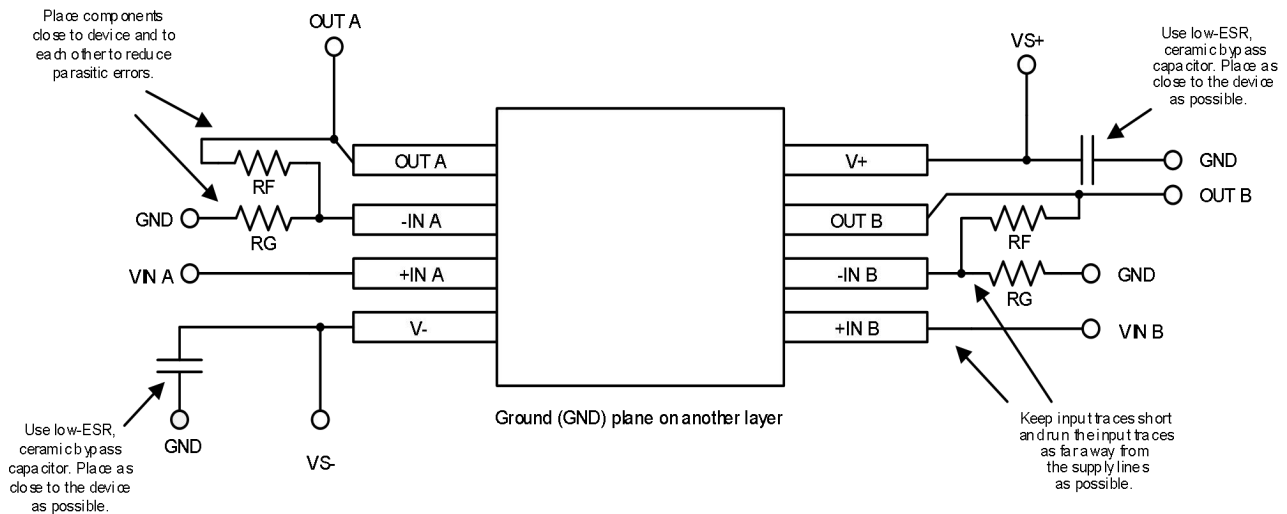
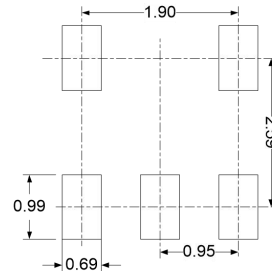
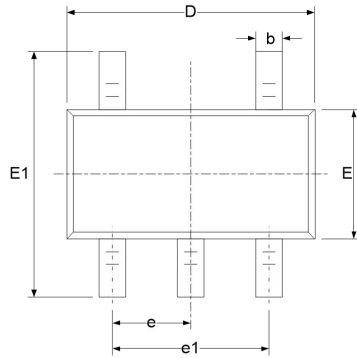


Figure 22. Layout Example

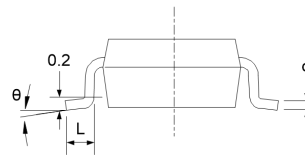
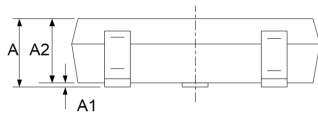


# 11 Pacakage Outline Dimensions

## SOT23-5



RECOMMENDED LAND PATTERN (Unit: mm)

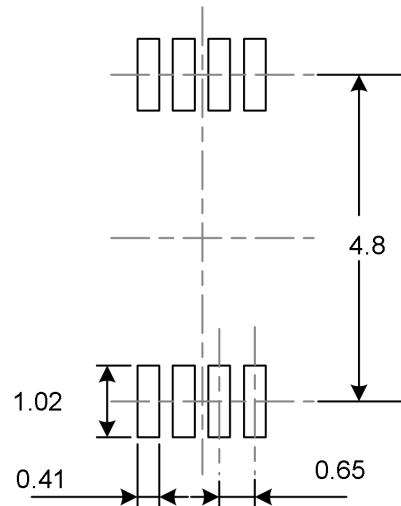
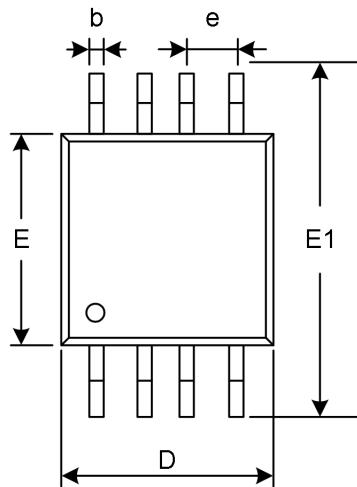


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°

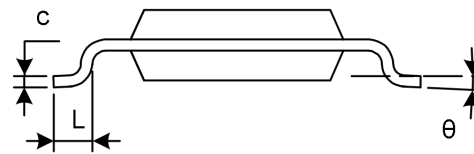
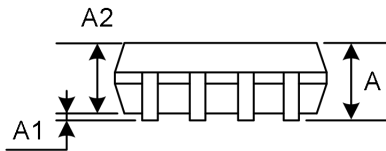
NOTE:

- A. This drawing is subject to change without notice.
- B. Plastic or metal protrusions of 0.15mm maximum per side are not included.
- C. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

MSOP-8



RECOMMENDED LAND PATTERN (Unit: mm)

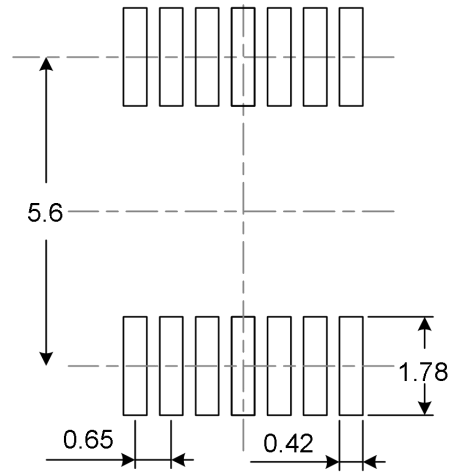
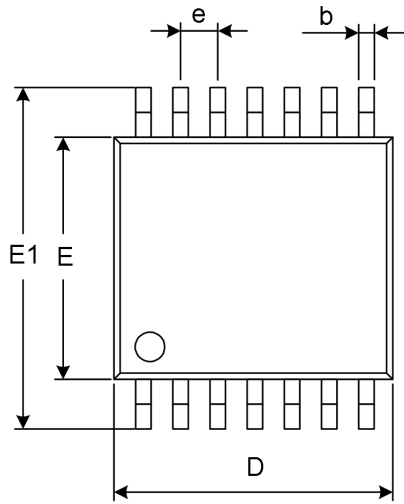


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
$\theta$	0°	6°	0°	6°

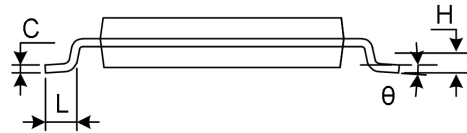
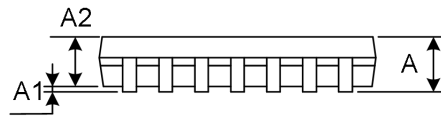
NOTE:

- A. This drawing is subject to change without notice.
- B. Plastic or metal protrusions of 0.15mm maximum per side are not included.
- C. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

TSSOP-14



RECOMMENDED LAND PATTERN (Unit: mm)

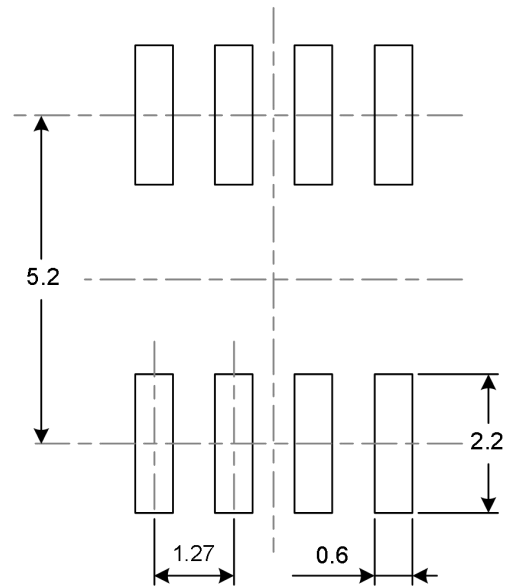
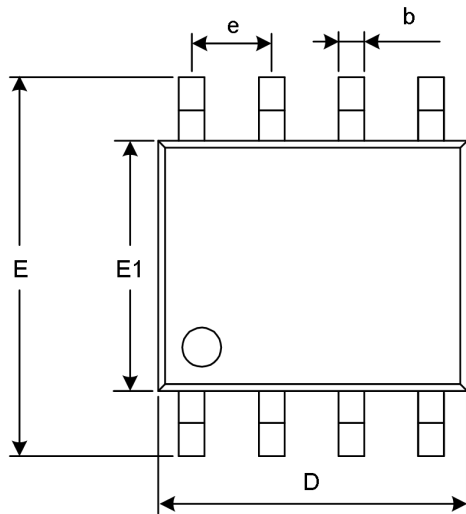


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
$\theta$	1°	7°	1°	7°

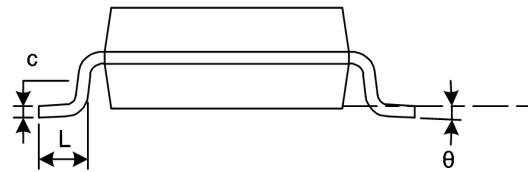
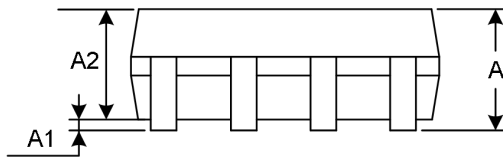
NOTE:

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- C. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

SOIC-8 (SOP8)



RECOMMENDED LAND PATTERN (Unit: mm)

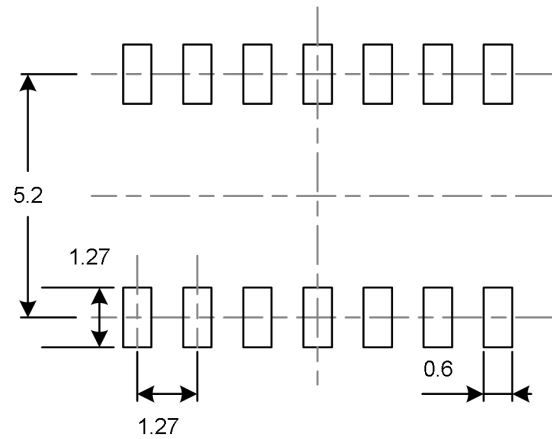
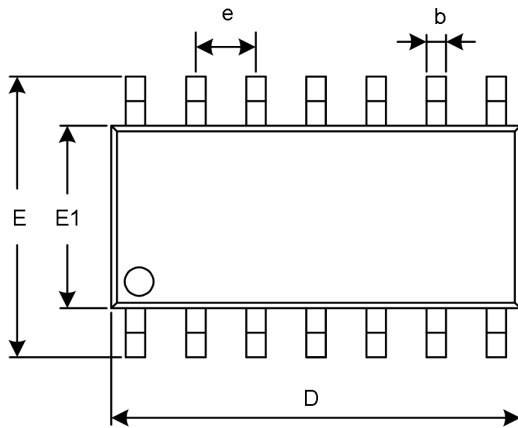


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

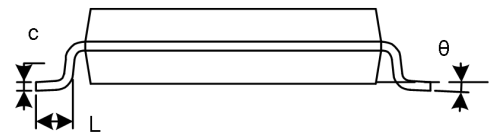
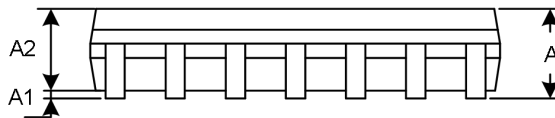
NOTE:

- A. This drawing is subject to change without notice.
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- C. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

SOIC-14 (SOP14)



RECOMMENDED LAND PATTERN (Unit: mm)



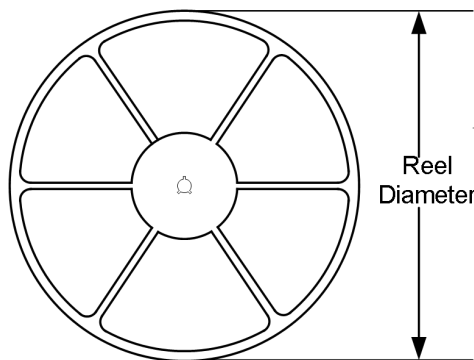
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

NOTE:

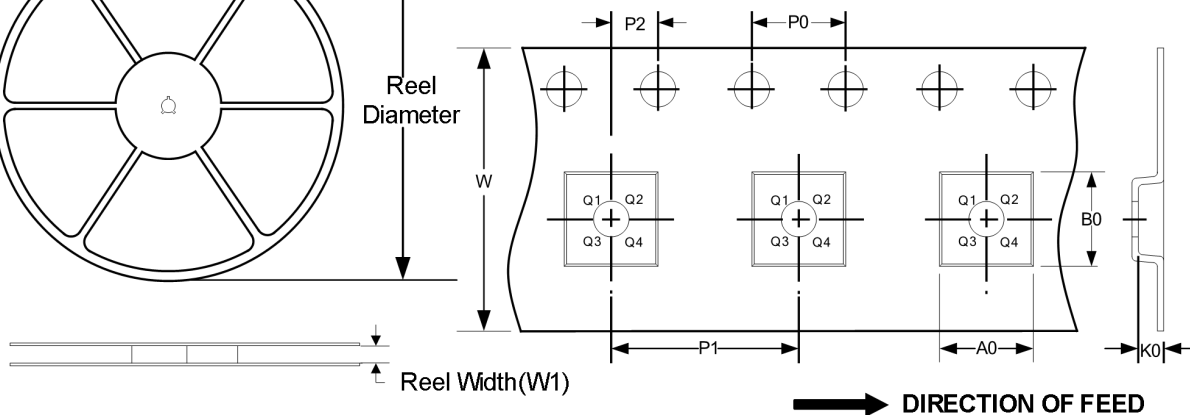
- A. This drawing is subject to change without notice.
- B. Plastic or metal protrusions of 0.15mm maximum per side are not included.
- C. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

## 12 Tape and Reel Information

### REEL DIMENSIONS



### TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TSSOP-14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOIC-8 (SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOIC-14 (SOP14)	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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