Zero-Drift, Low Power, CMOS Operational Amplifiers

1 Features

- **Input Offset Voltage: ±7μV (TYP)**
- **Input Offset Drift: ±0.08μV/°C**
- **Low Quiescent Current: 40μA/Amp**
- **Gain Bandwidth:350kHz**
- **Rail to Rail Input and Output**
- **Low Noise: 0.9μV_{P-P} (0.1Hz to 10Hz)**
- **Slew Rate:0.16V/μs**
- **Supply Range: 2V to 5.5V**
- **Extended Temperature: -40°C to +125°C**
- **Micro SIZE PACKAGES: SOT23-5, SOT353(SC70-5)**

2 Applications

- **Battery Powered Instruments**
- **Medical Instruments**
- **Handheld Test Equipment**
- **Temperature Measurements**
- **Transducers**
- **Electronic Scales**

3 Descriptions

The ZM8541, ZM8542 series of CMOS operational amplifiers use auto-calibration techniques to simultaneously provide very low offset voltage (7uV TYP) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With gain-bandwidth product of 350KHz and slew rate of 0.16V/us. Single or dual supplies as low as +2V (±1V) and up to +5.5V (±2.75V) may be used.

The ZM854X are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The ZM8541 single amplifier is available in 5-lead SOT23 and SOT353(SC70-5) packages, The ZM8542 dual amplifier is available in 8-lead SOIC and 8-lead MSOP packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
ZM8541	SOT23-5(5)	2.92mm×1.60mm
	SOT353 (SC70-5)	2.10mm×1.25mm
ZM8542	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/08/24	Initial version completed

5 Package/Ordering Information (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
ZM8541XF	SOT23-5	5	1	-40°C ~125°C	8541	MSL3	Tape and Reel,3000
ZM8541BXC5	SC70-5	5	1	-40°C ~125°C	8541B	MSL3	Tape and Reel,3000
ZM8542XK	SOIC-8(SOP8)	8	2	-40°C ~125°C	ZM8542	MSL3	Tape and Reel,4000
ZM8542XM	MSOP-8	8	2	-40°C ~125°C	ZM8542	MSL3	Tape and Reel,4000

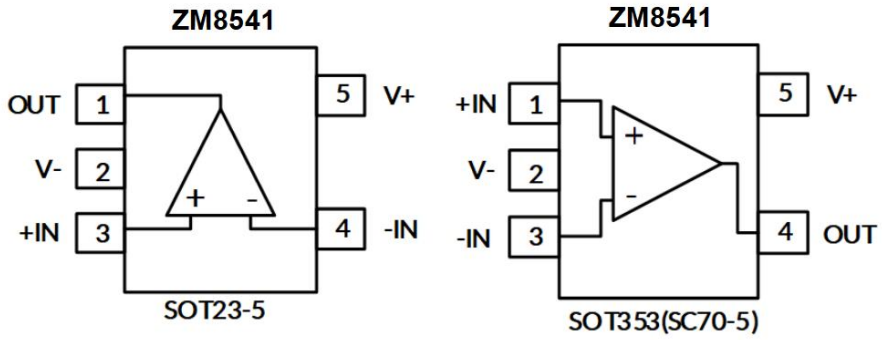
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) The MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F.

6 Pin Configuration and Functions (Top View)

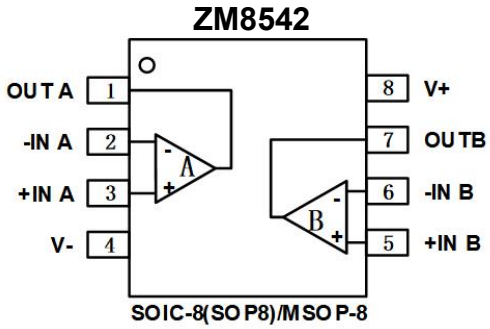


Pin Description

NAME	PIN		I/O (1)	DESCRIPTION
	ZM8541	ZM8541B		
	SOT23-5	SOT353(SC70-5)		
-IN	4	3	I	Negative (inverting) input
+IN	3	1	I	Positive (noninverting) input
OUT	1	4	O	Output
V-	2	2	-	Negative (lowest) power supply
V+	5	5	-	Positive (highest) power supply

(1) I = Input, O = Output.

Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O (1)	DESCRIPTION
	ZM8542		
	SOIC-8(SOP8)/MSOP-8		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

(1) I = Input, O = Output.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)			7	V
	Signal input pin (2)		(V-)-0.3	(V+) +0.3	
	Signal output pin (3)		(V-)-0.3	(V+) +0.3	
Current	Signal input pin (2)		-10	10	mA
	Signal output pin (3)		-10	10	mA
	Output short-circuits (4)		Continuous		
θ_{JA}	Package thermal impedance (5)	SOT23-5		230	°C/W
		SOIC-8(SOP8)		110	
		MSOP-8		165	
		SOT353/(SC70-5)		380	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (6)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±10mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±4000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115C (2010)	±300	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S= (V+) - (V-)	Single-supply	2		5.5	V
	Dual-supply	±1		±2.75	
Specified temperature		-40		125	°C

7.4 Electrical Characteristics

Boldface limits apply over the specified temperature range, Full [9] = -40°C to +125°C.
(At T_A = +25°C, V_S=5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, V_{CM} = V_S/2, unless otherwise noted.) [1]

PARAMETER		CONDITIONS	ZM854X			
			MIN [2]	TYP [3]	MAX [2]	UNIT
POWER SUPPLY						
V_S	Operating Voltage Range		2		5.5	V
I_Q	Quiescent Current Per Amplifier			40	60	μA
PSRR	Power-Supply Rejection Ratio	V_S=2 V to 5.5V	95	110		dB
INPUT						
V_{OS}	Input Offset Voltage	V_S= 2V, V_{CM}=V_S/2	-30	±3	30	μV
		V_S= 5V, V_{CM}=V_S/2	-30	±7	30	μV
V_{OS} T_C	Input Offset Voltage Average Drift			±0.08		μV/°C
IB	Input Bias Current [4] [5]	V_{CM} = V_S/2		±330		pA
I_{OS} [5]	Input Offset Current	V_{CM} = V_S/2		±100		pA
V_{CM}	Common-Mode Voltage Range		(V-)-0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	(V-)-0.1V<V_{CM}<(V+)+0.1V	105	120		dB
INPUT CAPACITANCE						
	Differential [5]			2.5		pF
	Common-Mode [5]			5		pF
OUTPUT						
A_{OL}	Open-Loop Voltage Gain	R_L=10KΩ, V_O= 0.3V to 4.7V	105	130		dB
V_{OL}	Output Voltage Low from rail	R_L=100 KΩ to GND		1		mV
		R_L=10 KΩ to GND		10	20	
V_{OH}	Output Voltage High from rail	R_L=100 KΩ to V+		1		mV
		R_L=10 KΩ to V+		10	20	
I_{SC}	Output Short-Circuit Current [6] [7]		±20	±30		mA
FREQUENCY RESPONSE						
SR	Slew Rate [8]	G=+1		0.16		V/μs
GBW	Gain-Bandwidth Product			350		KHz
t_{OR}	Overload Recovery Time	V_{IN}·Gain≥V_S		3		μs
NOISE PERFORMANCE						
e_np-p	Input Voltage Noise	f= 0.1Hz to 10Hz		0.9		$μV_{PP}$
e_np-p	Input Voltage Noise [5]	f= 0.01Hz to 1Hz		0.25		$μV_{PP}$
e_n	Input Voltage Noise Density [5]	f = 1KHz		45		$nV/\sqrt{Hz}$

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - T_A) / $R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25℃, V_S=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.

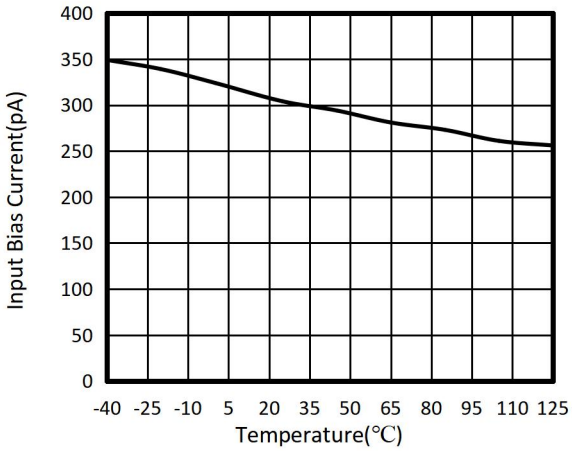


Figure 1. Input Bias Current vs Temperature

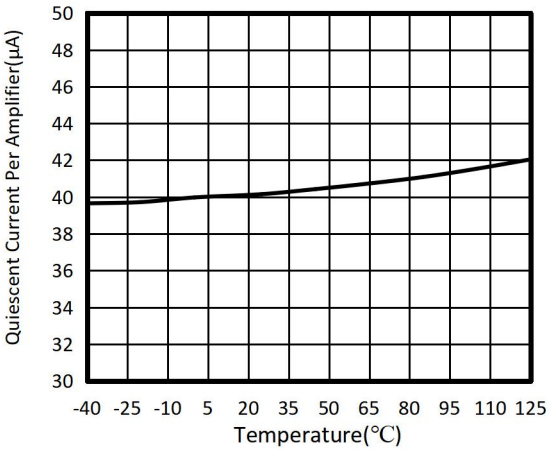


Figure 2. Quiescent Current vs Temperature

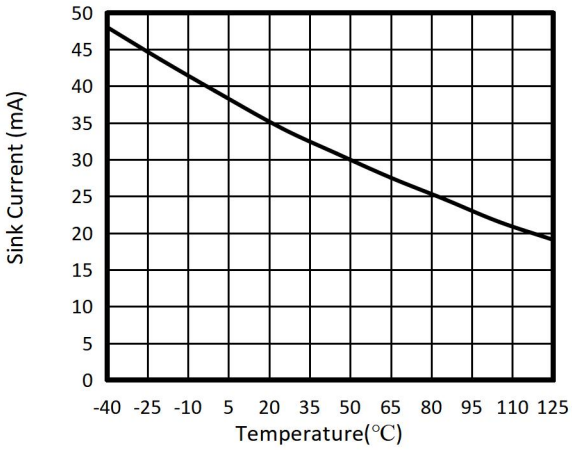


Figure 3. Sink Current vs Temperature

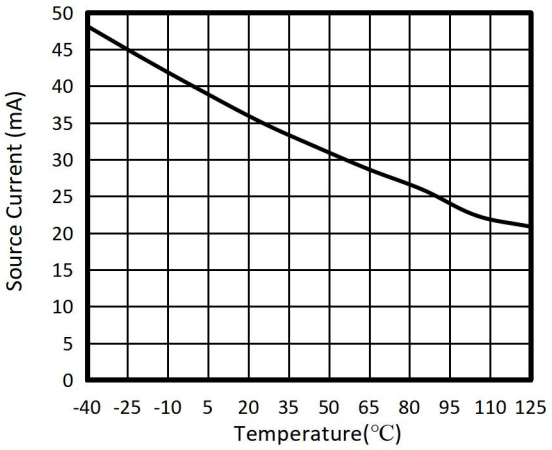


Figure 4. Source Current vs Temperature

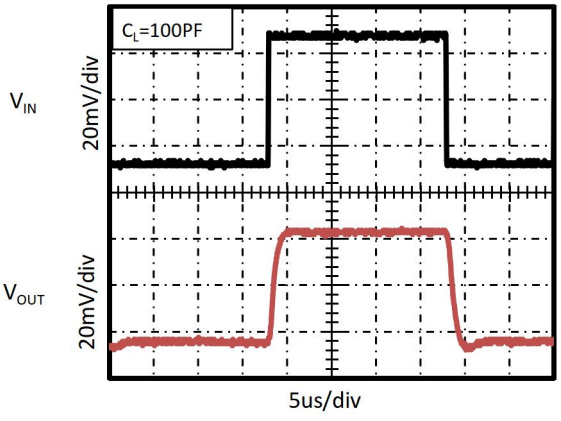


Figure 5. Small-Signal Step Response

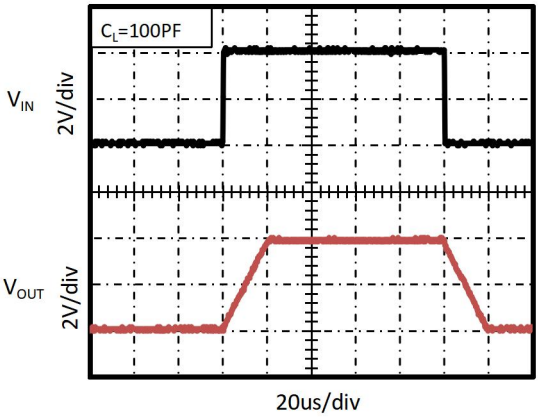


Figure 6. Large-Signal Step Response

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25℃, V_S=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.

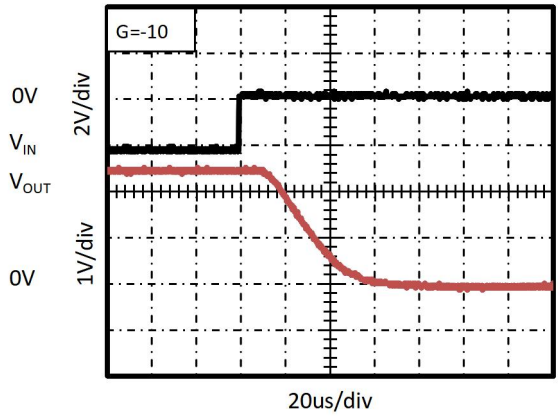


Figure 7. Positive Overvoltage Recovery

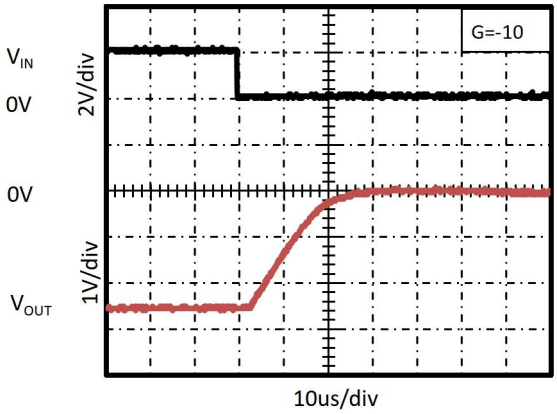


Figure 8. Negative Overvoltage Recovery

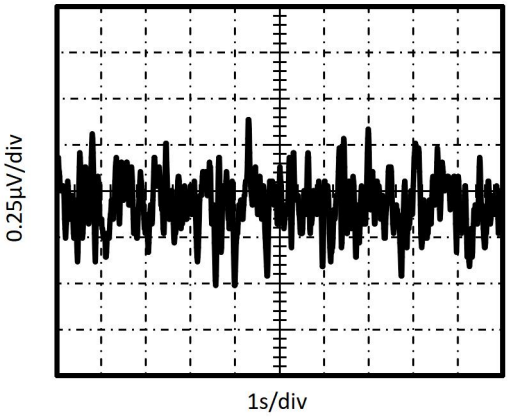


Figure 9. 0.1Hz to 10Hz Noise

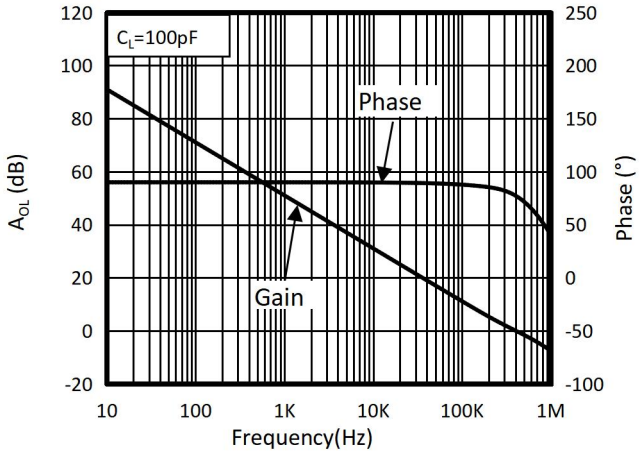


Figure 10. Open−Loop Gain and Phase vs Frequency

8 Detailed Description

8.1 Overview

The ZM854X is a family of Zero-Drift, low-power, rail-to-rail input and output operational amplifiers. These devices operate from 2 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The Zero-Drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

8.2 Feature Description

The ZM854X series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1uF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1uV/°C or higher, depending on materials used.

8.3 Operating Voltage

The ZM854X series op amps operate over a power-supply range of +2V to +5.5V (±1V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

8.4 Device Functional Modes

The ZM854X device has a single functional mode. The device is powered on as long as the power supply voltage is between 2 V (±1 V) and 5.5 V (±2.75 V).

9 Application and Implementation

Information in the following applications sections is not part of the Z-Micro component specification, and Z-Micro does not warrant its accuracy or completeness. Z-Micro's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 APPLICATION NOTE

The ZM854X is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1uF capacitors are adequate.

9.2 Typical Applications

9.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from -1 A to 1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the ZM854X because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other provides the reference voltage.

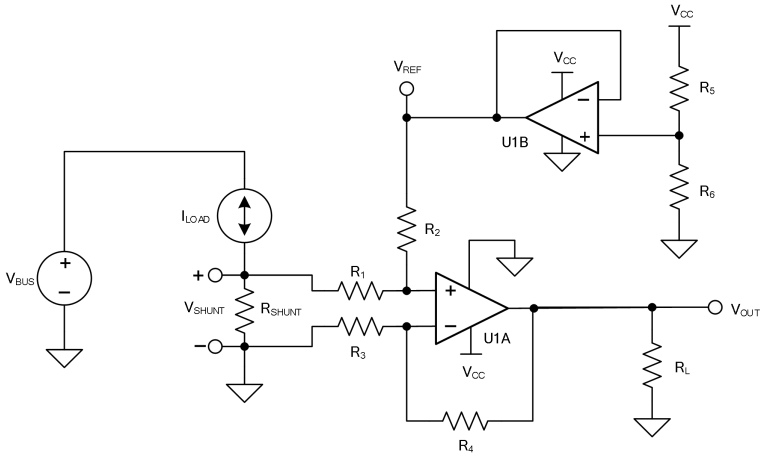


Figure 11. Bidirectional Current-Sensing Schematic

9.2.2 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: -1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

9.2.3 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$V_{OUT}=V_{SHUNT}\times Gain_{Diff\_Amp}+V_{REF}$

Where

$V_{SHUNT}=I_{LOAD}\times R_{SHUNT}$

$$Gain_{Diff\_Amp}=\frac{R_4}{R_3}$$

$$V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right) \quad (1)$$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value impacts the CMRR of the difference amplifier, which ultimately translates to an offset error. Because this is a low-side measurement, the value of V_{SHUNT} is the ground potential for the system load. Therefore, it is important to place a maximum value on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is -100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, it is important to use an operational amplifier, such as the ZM854X, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the ZM854X has a typical offset voltage of ±2uV (±10uV maximum). Given a symmetric load current of -1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used. To set the gain of the difference amplifier, the common-mode range and output swing of the ZM854X must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the ZM854X given a 3.3-V supply.

$-100mV<V_{CM}<3.4V$ (3)

$100mV<V_{OUT}<3.2V$ (4)

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1A)]} = 15.5\ \frac{V}{V} \quad (5)$$

The resistor value selected for R_1 and R_3 was 1kΩ. 15.4kΩ was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

9.2.4 Application Curve

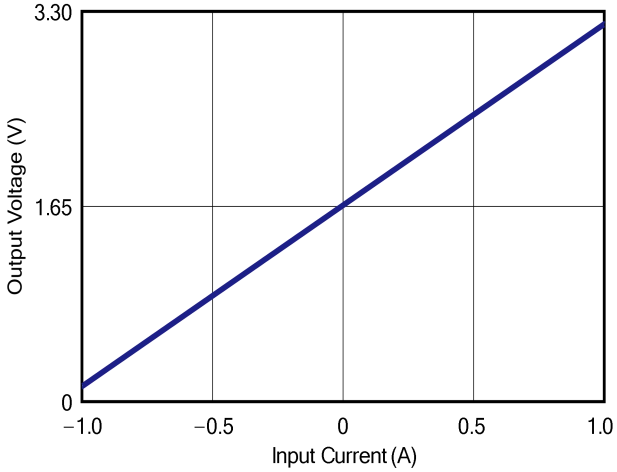


Figure 12. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

10.2 Layout Example

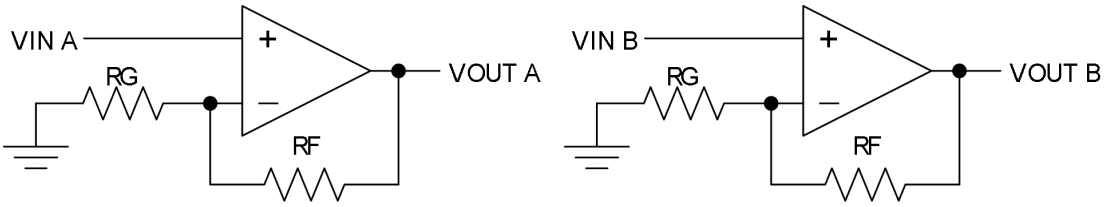
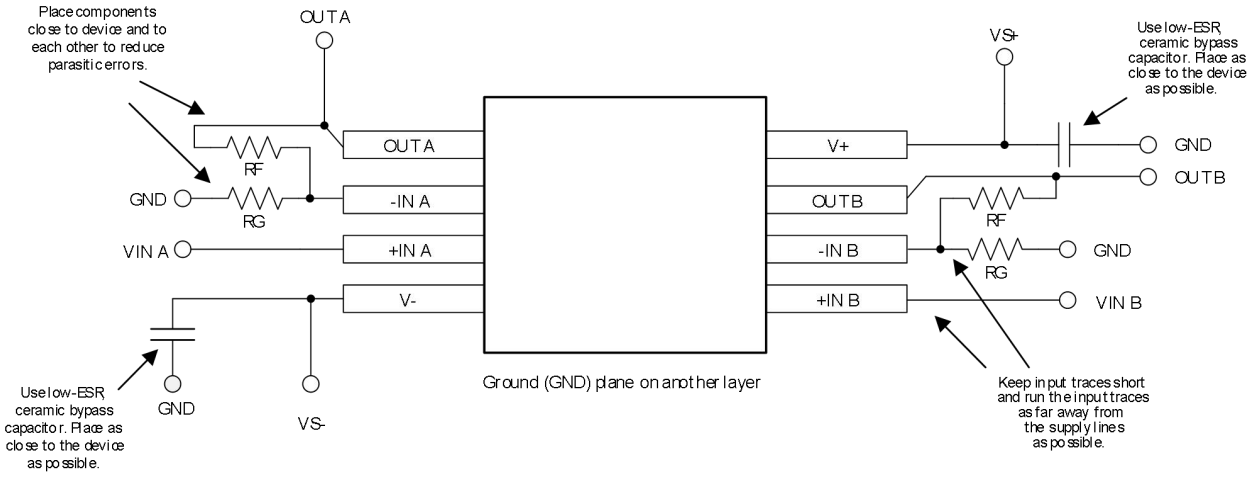


Figure 13. Schematic Representation



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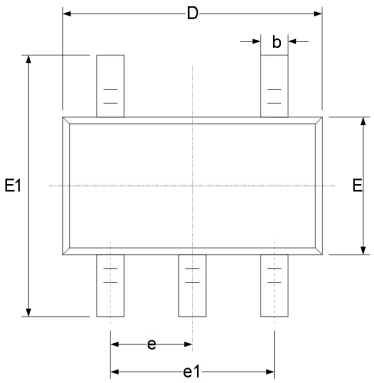
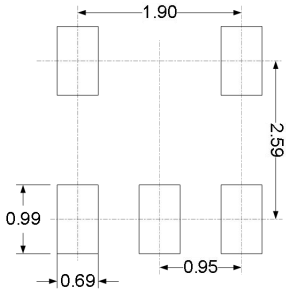
igure 14. Layout Example

NOTE: Layout Recommendations have been shown for dual op-amp only, follow similar precautions for Single and four.

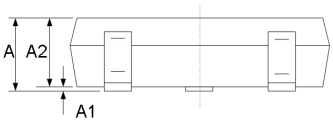
11 Package Outline Dimensions

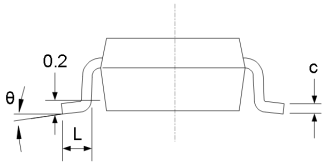
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



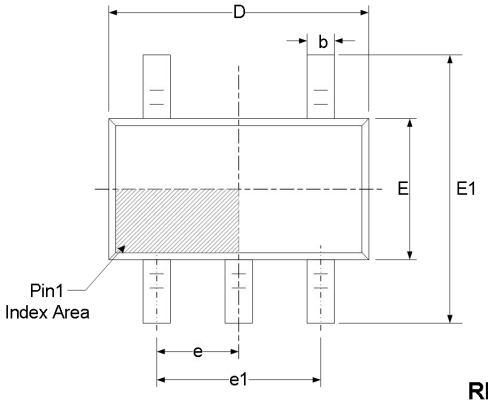


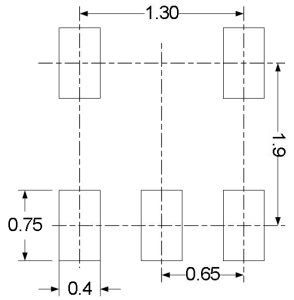
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

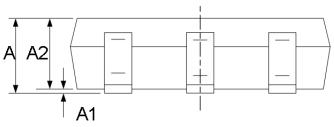
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

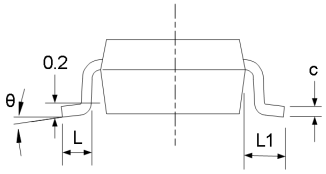
SOT353(SC70-5) [3]





RECOMMENDED LAND PATTERN (Unit: mm)



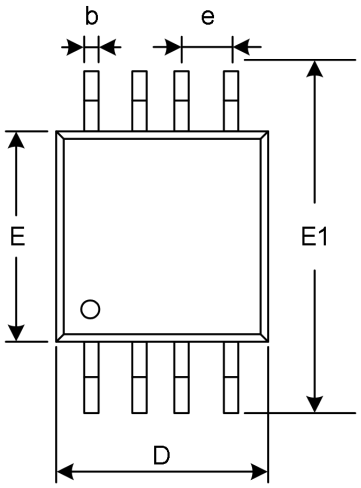


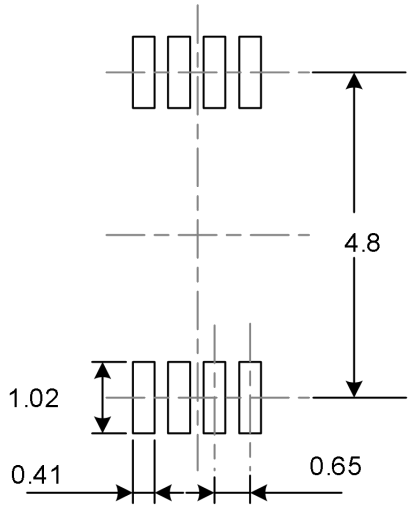
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A [1]	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D [1]	2.000	2.200	0.079	0.087
E [1]	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) [2]		0.026(BSC) [2]	
e1	1.300(BSC) [2]		0.051(BSC) [2]	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

NOTE:

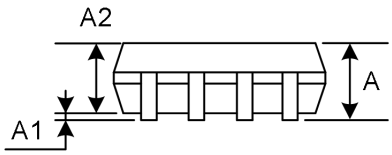
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

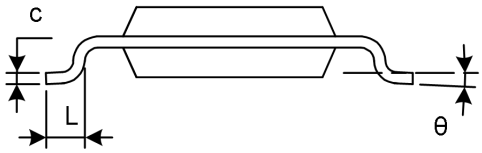
MSOP-8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



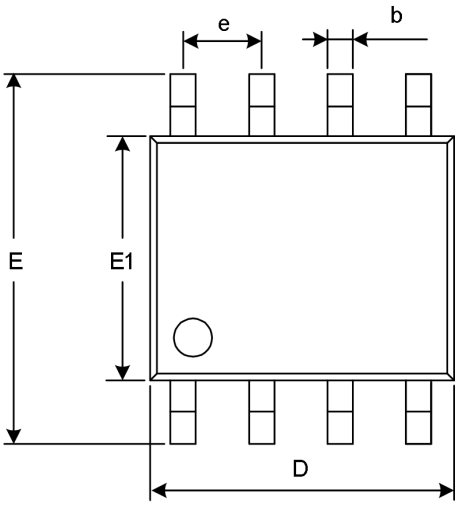


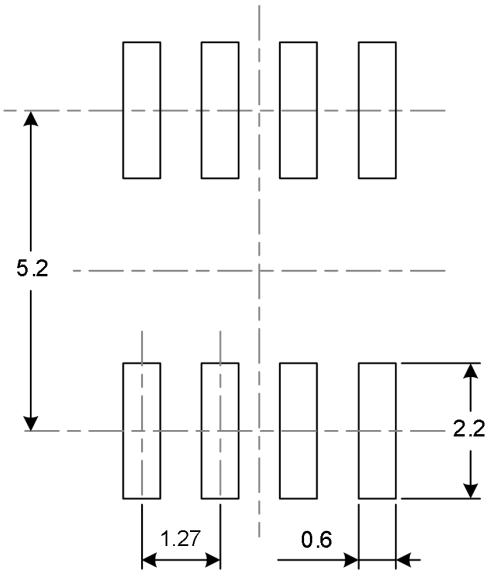
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

NOTE:

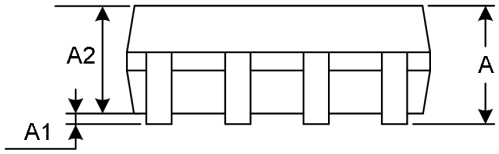
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

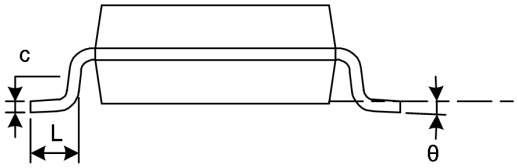
SOIC-8(SOP8) [3]





RECOMMENDED LAND PATTERN (Unit: mm)





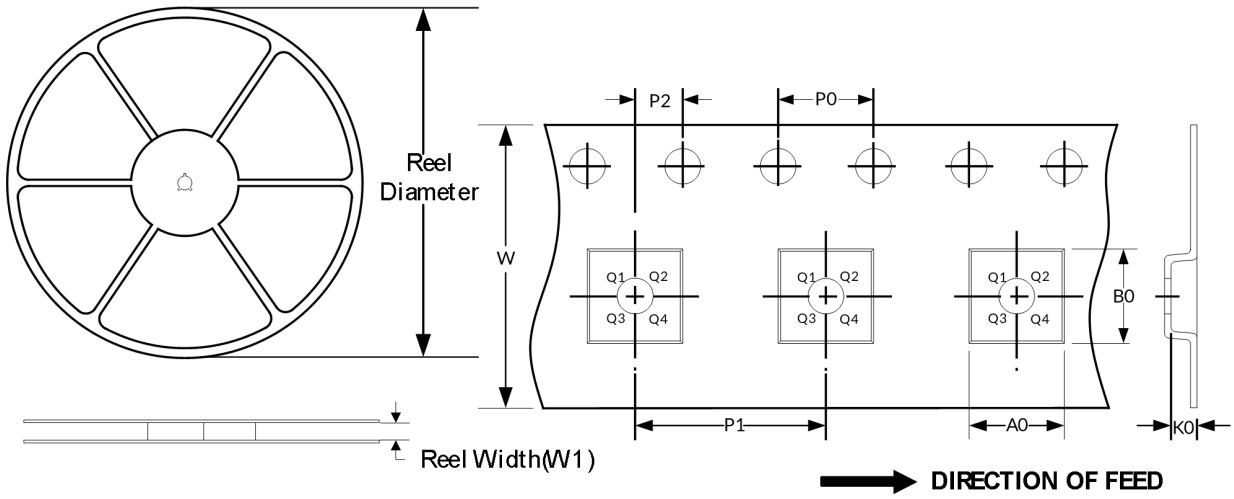
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A [1]	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D [1]	4.800	5.000	0.189	0.197
e	1.270(BSC) [2]		0.050(BSC) [2]	
E	5.800	6.200	0.228	0.244
E1 [1]	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 Tape and Reel Information

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7''	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT353(SC70-5)	7''	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3
SOIC-8(SOP8)	13''	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13''	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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